Koneru Lakshmaiah Education Foundation
(Category -1, Deemed to be University estd. u/s. 3 of the UGC Act, 1956)
Accredited by NAAC as 'A++' ◆Approved by AICTE ◆ ISO 9001-2015 Certified
Campus: Green Fields, Vaddeswaram - 522 302, Guntur District, Andhra Pradesh, INDIA.
Phone No. 08645 - 350200; www.klef.ac.in; www.klef.edu.in; www.kluniversity.in
Admin Off: 29-36-38, Museum Road, Governorpet, Vijayawada - 520 002. Ph: +91 - 866 - 3500122, 2576129.

Ref: KLEF/RO/ECE/CIRCULAR **Date: 14-07-2022**

CIRCULAR

Sub: Organizing event "Workshop" for the students of Electronics and Communication Engineering, of Vaddeswaram Campus of KLEF – Reg.

***

This is to inform that the Department of Electronics and Communication Engineering, KLEF, is Organizing a "Workshop on Digital VLSI Design: Logic Synthesis and Verification" for the students of Electronics and communication Engineering, Vaddeswaram Campus of KLEF on, 16-07-2022, as details below:

Event Name: "Workshop"
Date: 16-07-2022
Venue: R-106

All the students of ECE, are invited to attend this program.
Dy-HOD's & Year coordinators are requested to bring this information to the attention of all ECE students and encourage them to participate in this program.

HOD-ECE
Dr.M.Suman

To
All ECE Students,
All ECE Faculty,
Principal.

Koneru Lakshmaiah Education Foundation
(Category -1, Deemed to be University estd. u/s. 3 of the UGC Act, 1956)
Accredited by NAAC as 'A++' ❖Approved by AICTE ❖ ISO 21001:2018 Certified
Campus: Green Fields, Vaddeswaram - 522 302, Guntur District, Andhra Pradesh, INDIA.
Phone No. +91 8645 - 350 200; www.klef.ac.in; www.klef.edu.in; www.kluniversity.in
Admin Off: 29-36-38, Museum Road, Governorpet, Vijayawada - 520 002. Ph: +91 - 866 - 3500122, 2576129

A Three-Day Workshop On "Digital VLSI Design: Logic Synthesis and Verification"

By

Always@VLSI

Department Of ECE

Name of the event: Digital VLSI Design: Logic Synthesis and Verification

Dates: 16-07-2022

Venue: R106

No. of students participated: 47

Objective of the event:

The outcome of the workshop "Digital VLSI Design: Logic Synthesis and Verification" is participants who are proficient in the principles, methodologies, and tools essential for successful digital VLSI design. Through hands-on exercises, practical demonstrations, and discussions on advanced techniques and best practices, attendees will gain a deep understanding of logic synthesis and verification processes. They will be equipped with the knowledge and skills necessary to efficiently design, synthesize, and verify digital circuits, ensuring correctness, performance, and reliability. Additionally, participants will be able to leverage industry-standard tools and methodologies to optimize design productivity, meet design specifications, and adhere to design constraints. Overall, the workshop will empower participants to excel in digital VLSI design, delivering high-quality digital circuits that meet stringent performance, power, and area requirements.

Description of the event:

The workshop "Digital VLSI Design: Logic Synthesis and Verification" offers a comprehensive exploration of the principles, methodologies, and tools essential for successful

digital VLSI design. Participants will delve into the intricacies of logic synthesis and verification processes, gaining practical insights and hands-on experience in key areas such as RTL design, logic optimization, synthesis, and functional verification. Led by experienced VLSI designers and industry experts, the workshop covers a wide range of topics, including HDL-based design, design constraints, timing analysis, and testbench development. Emphasis is placed on industry-standard tools and methodologies, enabling participants to efficiently design, synthesize, and verify digital circuits while meeting stringent performance, power, and area requirements.

Throughout the workshop, participants will engage in interactive sessions, practical demonstrations, and collaborative exercises, allowing them to apply theoretical concepts to real-world design challenges. They will gain proficiency in industry-standard design and verification tools such as Cadence Encounter, Synopsys Design Compiler, and Mentor Graphics ModelSim, enhancing their ability to develop high-quality digital designs efficiently. Additionally, participants will learn best practices for design optimization, verification planning, and debugging, ensuring correctness, reliability, and scalability in their digital designs. By the end of the workshop, participants will emerge with a comprehensive skill set, equipped with the knowledge, tools, and methodologies necessary to excel in digital VLSI design, delivering innovative and high-performance digital circuits that meet the demands of modern semiconductor technologies.

Outcome of the event:

Overall, the outcome of the workshop will be participants who are well-equipped with the knowledge, skills, and tools necessary to excel in digital VLSI design. They will be capable of developing innovative and high-performance digital circuits that meet the demands of modern semiconductor technologies, contributing to advancements in the field of digital integrated circuit design. Proficiency in Design Tools: Participants will gain proficiency in industry-standard digital VLSI design and verification tools such as Cadence Encounter, Synopsys Design Compiler, and Mentor Graphics ModelSim. This proficiency will enable them to efficiently design, synthesize, and verify digital circuits while adhering to design constraints and meeting performance targets. Deep Understanding of Methodologies: Attendees will develop a deep understanding of digital VLSI design methodologies, including RTL design, logic synthesis, optimization techniques, and functional verification strategies.

This understanding will empower participants to apply the most appropriate methodologies and techniques to their design projects effectively. Enhanced Problem-Solving Skills: Through hands-on exercises and practical demonstrations, participants will sharpen their problem-solving skills, learning how to address common challenges and complexities encountered in digital VLSI design. This will enable them to develop robust and reliable digital circuits that meet design specifications and requirements. Quality Assurance: Participants will learn best practices for functional verification, timing analysis, and testbench development, ensuring the correctness, reliability, and scalability of their digital designs. This emphasis on quality assurance will help participants deliver high-quality digital circuits that meet industry standards and customer expectations. Optimized Design Productivity: Armed with a comprehensive understanding of digital VLSI design principles and methodologies, participants will be able to optimize design productivity and efficiency. They will learn how to streamline the design process, minimize design iterations, and maximize design reuse, ultimately reducing time-to-market and development costs.

photos of the event:

Mentor explaining the logic synthesis

Participant's List:

S. NO	STUDENT ID	STUDENT NAME	DEPT	SIGNATURE
1.	2100049095	ALETI SANTHOSH .	ECE	
2.	2100049084	JALDU MOUNIKA NAGA RAMA SUDHA	ECE	
3.	2100049082	MEDISETTI GUNASRI	ECE	
4.	2100049081	MALE SAI MANIKANTA	ECE	
5.	2100049080	TALLA VENKATA GOPI ROHITH	ECE	
6.	2100049079	VELAMARTHI ABHINAY ANAND	ECE	
7.	2100049077	VEERAMACHANENI VENKATA NAVEEN	ECE	
8.	2100049076	YANAMALAMANDA VAMSI	ECE	
9.	2100049072	CHEEPURUPALLI BALA SRIDHAR	ECE	
10.	2100049071	ADIREDDY JYOTHI BHAVANI SHANKAR	ECE	
11.	2100049068	JANGILI SIVA SAI PRAKASH	ECE	
12.	2100049065	UPPALA RAVI TEJA	ECE	
13.	2100049064	POKALA SURYA AKASH	ECE	
14.	2100049063	PRUDHVI GOPAL VELISALA	ECE	
15.	2100049051	SYED ASHRUF	ECE	
16.	2100049050	MADEM SIVA MASTHAN REDDY	ECE	
17.	2100049047	KORIVI AKHIL	ECE	
18.	2000049032	KUCHIPUDI LAKSHMI MANJU PRAVALLIKA	ECE	
19.	2000049031	GEDELA YASHWANTH SAIRAM	ECE	

20.	2000049029	KUNDELLA GANESH YADAV	ECE	Ganesh
21.	2000049028	MYNAMPATI VENKATA SAI SRI PRABHAS	ECE	Prabhas
22.	2000049026	SRIPATHI CHANDANA	ECE	Chanda
23.	2000049022	KRAPA LOKESH	ECE	Lokesh O.
24.	2000049019	VYSHNAVI VIPPAGUNTA	ECE	V. vaishnavi
25.	2000049016	JINKA JITENDRA SAI KARTHIK	ECE	Sai Karthik.
26.	2000049015	YADALA VENKATA NITHISH KUMAR	ECE	Y.V. Nithish
27.	2000049013	GUDURU BALAJI INDUJA	ECE	Induja
28.	2000049045	CHAPARALA TEJA SRI	ECE	TejaSri
29.	2000049041	MELAM VEERA SAI TEJA	ECE	M. VeeraSaiTeja
30.	2000040281	VANTEDDU PRAVEEN REDDY	ECE	V. praveen.
31.	2000040273	GAYATHRI KETINENI	ECE	Gayathri
32.	2000040272	APPANI GOPICHANDU	ECE	gopichand
33.	2000040270	PODURI ABHISHEK SURYA	ECE	Surya O.
34.	2000040269	MANOJ KUMAR ROKKAM	ECE	K. Manoj
35.	2000040268	GANDREDDI CHAITANYA NAIDU	ECE	Chaitanya
36.	2000040266	BOJJA SIVA VAISHNAVI	ECE	Vaishnavi
37.	2000040261	MALISETTY ROHAN	ECE	Rohan
38.	2000040258	PATHAN HASAN ZAHEERKHAN	ECE	Zaheer Khan
39.	2000040256	NALI BHARGAVA SARASWATHI	ECE	N. Bhargava.
40.	2000040252	KOTA LAKSHMI MANOGNA	ECE	Manogna
41.	2000040249	BODDOJU VISHNU VARDHAN	ECE	B. Vishnu.
42.	2000040245	GURRAMPATI PREETHI REDDY	ECE	Preethi.

43.	2000040244	VISHNU VARDHAN REDDY	ECE	
44.	2000040196	RAJARIKAM KIREETI	ECE	
45.	2000040193	KANAMARLAPUDI VENKATA SURYA	ECE	
46.	2000040187	VALLAMKONDA SATVIKA	ECE	
47.	2000040184	SURALA DEVA VENKATA SAI	ECE	

In charge
Always@VLSI Technical Club
Mr S. Vamsee Krishna

HOD/ECE
Dr. M. Suman

Dr. M. SUMAN
Professor & Head
Department of ECE
K L E F
Green Fields, Vaddeswaram
Guntur Dist., A.P. PIN- 522 502