Koneru Lakshmaiah Education Foundation
(Category -1, Deemed to be University estd. u/s. 3 of the UGC Act, 1956)
Accredited by NAAC as 'A++' ❖ Approved by AICTE ❖ ISO 21001:2018 Certified
Campus: Green Fields, Vaddeswaram - 522 302, Guntur District, Andhra Pradesh, INDIA.
Phone No. +91 8645 - 350 200; www.klef.ac.in; www.klef.edu.in; www.kluniversity.in
Admin Off: 29-36-38, Museum Road, Governorpet, Vijayawada - 520 002. Ph: +91 - 866 - 3500122, 2576129

Ref: KLEF/RO/ECE/CIRCULAR **Date: 02-08-2020**

CIRCULAR

Sub: Organizing event "Workshop" for the students of Electronics and Communication Engineering, of Vaddeswaram Campus of KLEF – Reg.

***

This is to inform that the Department of Electronics and Communication Engineering, KLEF, is Organizing a "Workshop on ASIC Design Flow: Methodologies and Best Practices" for the students of Electronics and communication Engineering, Vaddeswaram Campus of KLEF on, 05-08-2020, as details below:

Event Name: "Workshop"
Date: 05-08-2020
Venue: R-106

All the students of ECE, are invited to attend this program.
Dy-HOD's & Year coordinators are requested to bring this information to the attention of all ECE students and encourage them to participate in this program.

HOD-ECE
Professor & Alternate HO.
Department of ECE
K L University
VADDESWARAM
Guntur Dt., A.P., India

To
All ECE Students,
All ECE Faculty,
Principal.

Koneru Lakshmaiah Education Foundation
(Category -1, Deemed to be University estd. u/s. 3 of the UGC Act, 1956)
Accredited by NAAC as 'A++' ❖Approved by AICTE ❖ ISO 9001-2015 Certified
Campus: Green Fields, Vaddeswaram - 522 302, Guntur District, Andhra Pradesh, INDIA.
Phone No. 08645 - 350200; www.klef.ac.in; www.klef.edu.in; www.kluniversity.in
Admin Off: 29-36-38, Museum Road, Governorpet, Vijayawada - 520 002. Ph: +91 - 866 - 3500122, 2576129.

Expert talk On "ASIC Design Flow: Methodologies and Best Practices"

By

Always@VLSI

Department Of ECE

Name of the event: ASIC Design Flow: Methodologies and Best Practices

Dates:05-08-2020

Venue:R106

No. of students participated: 41

Objective of the event:

The objective of the workshop "ASIC Design Flow: Methodologies and Best Practices" is to provide participants with a comprehensive understanding of the Application-Specific Integrated Circuit (ASIC) design flow, encompassing methodologies and best practices crucial for successful ASIC development. Through interactive sessions, lectures, and practical exercises, participants will gain insights into each stage of the ASIC design flow, from specification and architecture definition to synthesis, verification, and tape-out. The workshop aims to equip participants with the knowledge, skills, and tools necessary to navigate the complexities of ASIC design effectively, enabling them to develop high-quality ASICs that meet performance, power, and area requirements while adhering to industry standards and best practices.

Description of the event:

The workshop "ASIC Design Flow: Methodologies and Best Practices" offers a comprehensive exploration of the Application-Specific Integrated Circuit (ASIC) design process, focusing on methodologies and best practices essential for successful ASIC development. Throughout the workshop, participants will delve into each stage of the ASIC

design flow, gaining practical insights and hands-on experience in key areas such as specification, architecture definition, design implementation, verification, and tape-out.

Led by experienced ASIC designers and industry experts, the workshop covers a wide range of topics, including RTL design, synthesis, timing analysis, design for testability (DFT), physical design, and post-silicon validation. Emphasis is placed on industry-standard tools, methodologies, and techniques, enabling participants to develop a deep understanding of ASIC design principles and apply them effectively in real-world projects. By the end of the workshop, participants will emerge with a comprehensive skill set, equipped with the knowledge, tools, and best practices necessary to navigate the complexities of ASIC design and deliver high-quality ASICs that meet performance, power, and area targets while adhering to industry standards and best practices. Whether participants are new to ASIC design or seasoned professionals, this workshop provides invaluable insights and practical guidance to enhance their expertise and proficiency in ASIC design methodologies and best practices.

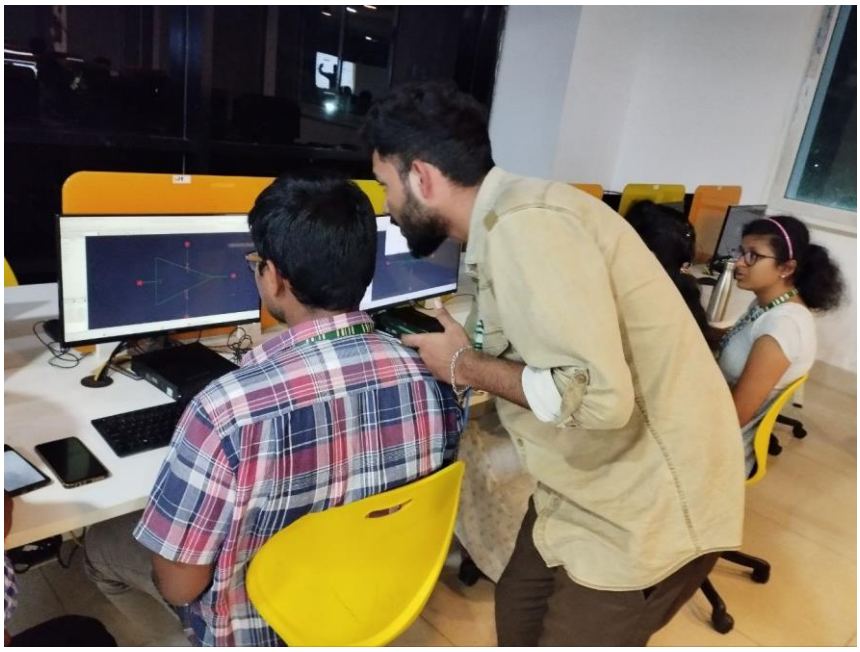
Outcome of the event:

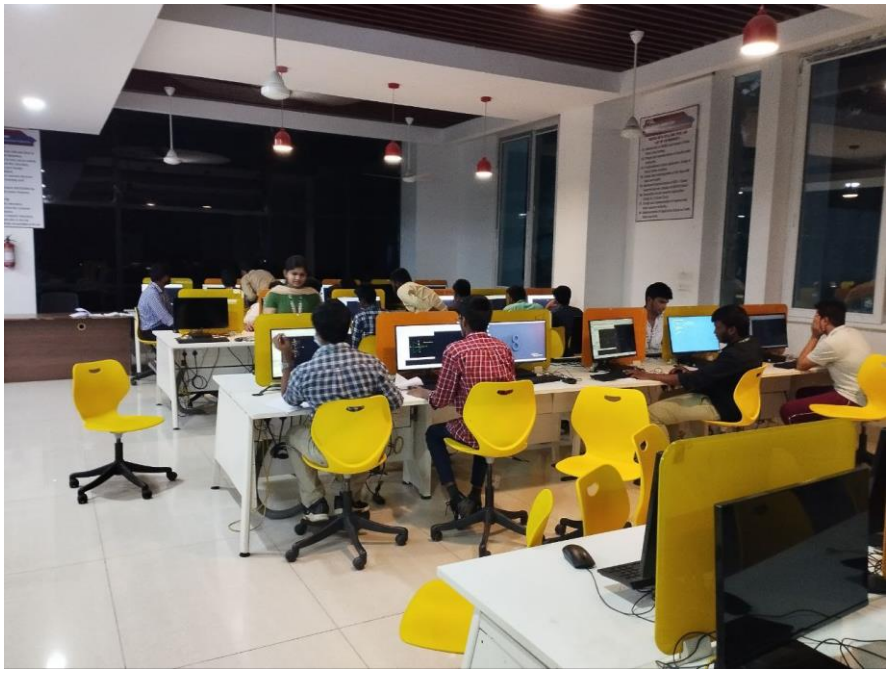
Comprehensive Understanding: Participants will gain a comprehensive understanding of the ASIC design flow, including methodologies and best practices essential for successful ASIC development. They will be equipped with in-depth knowledge of each stage of the design process, from specification and architecture definition to synthesis, verification, and tape-out.Proficiency in Design Tools: Attendees will become proficient in using industry-standard ASIC design tools and software, enabling them to effectively navigate the design flow and implement ASIC designs with precision and efficiency.Practical Skills: Through hands-on exercises and practical demonstrations, participants will develop practical skills in RTL design, synthesis, timing analysis, design for testability (DFT), physical design, and post-silicon validation, enhancing their ability to tackle real-world ASIC design challenges.

Adherence to Best Practices: Participants will learn industry best practices and guidelines for ASIC design, ensuring that their designs meet performance, power, and area targets while adhering to industry standards and requirements.Problem-Solving Abilities: By addressing common challenges and limitations encountered during ASIC design, participants will develop effective problem-solving abilities, enabling them to overcome design complexities and optimize ASIC designs for improved performance and reliability.

Quality Assurance: Through rigorous verification and validation techniques taught in the workshop, participants will ensure the correctness and reliability of their ASIC designs, minimizing the risk of errors and defects in the final product.Collaboration Opportunities: The workshop will provide opportunities for networking and collaboration with peers, industry experts, and practitioners in the field of ASIC design, fostering a supportive community and facilitating knowledge exchange.Enhanced Efficiency: Armed with a deep understanding of ASIC design methodologies and best practices, participants will be able to streamline the design process, reduce time-to-market, and improve overall design efficiency, resulting in more competitive ASIC products.Continued Learning: The workshop will serve as a foundation for continued learning and professional development in ASIC design, empowering participants to stay abreast of advancements in the field and adapt to evolving technologies and methodologies.Overall, the outcome of the workshop will be participants who are well-equipped with the knowledge, skills, and tools necessary to excel in ASIC design, delivering high-quality ASICs that meet performance, power, and area targets while adhering to industry standards and best practices.

Photos of the event:





Students working on ASIC design flow

Participant's List:

S. No	Name of the Student	Register Number	Branch	Signature
1.	180040698	KURUGUNTLA TANUJA	ECE	
2.	180040695	KALIDINDI NAVEEN	ECE	
3.	180040692	S V SIVA KISHORE	ECE	
4.	180040679	MANNEPALLI VENKATA RAMARAJU	ECE	
5.	180040662	GADDAM VAISHNAVI	ECE	
6.	180040647	PREMITHA CHEEMAKURTHI	ECE	
7.	180040645	CHINTAPOODI PAVANKALYAN	ECE	
8.	180040641	SANAGAVARAPU SAIKUMAR	ECE	
9.	180040635	ATMAKURI KAVYA	ECE	
10.	180040604	VASIREDDY BALASARASWATHI	ECE	
11.	180040590	POLURU JEEVAN REDDY	ECE	
12.	180040585	JAMPANI YUGESH	ECE	
13.	180040582	JALDU VENKATA NAGA SASIDHAR	ECE	
14.	180040579	VADDEMPUDI SONY	ECE	
15.	180040577	DURUGADDA VEERA JANARDHANA ACHARI	ECE	
16.	180040576	SIDDINENI POOJA NAIDU	ECE	
17.	180040556	SHAIK LUBNA KOWSAR	ECE	
18.	180040552	NALAMASA SUSHURUTH	ECE	
19.	180040546	PAKANATI A PAVAN KUMAR	ECE	
20.	180040542	KONDAMURI SRI VENKATA SHANMUKHA PRIYA	ECE	
21.	180040534	GUNDAVARAM VARSHITH RAO	ECE	
22.	180049020	SHAIK THAHERUNNISA	ECE	
23.	180049014	SINGAMSETTY LOHITH NAGA SAI BRAHMENDRA	ECE	
24.	180049012	KONAKATI SAI KIRAN	ECE	
25.	180049010	KADALI JAGADEESH	ECE	

26.	180049009	KILARU SAI PRASANTH	ECE	
27.	180049008	JAKKAMSETTI PAVAN PHANEENDRA MANIKUMAR	ECE	
28.	180049007	IRRINKI NAGA DURGA RAJESH	ECE	
29.	180049003	B SHIVA KUMAR	ECE	
30.	180040757	HARISH KUMAR DHARAVATH	ECE	
31.	180040743	MUDIYALA LOKESH REDDY	ECE	
32.	180040737	KADALI SAI SNEHA	ECE	
33.	180040726	MADENENI VENKAT CHANDU	ECE	
34.	180040721	MADHURI TAMMA	ECE	
35.	180040716	RANGISETTY LEELA KRISHNA	ECE	
36.	180040704	PERUMALLA GIRISH BABU	ECE	
37.	170041042	ELURI DHATHRI	ECE	
38.	170041040	PARASU SAI PRASANTHI	ECE	
39.	170041039	LAKKAKULA SAI SUMA	ECE	
40.	170041037	UPASI VENKATA KRISHNA CHAITANYA	ECE	
41.	180040698	KURUGUNTLA TANUJA	ECE	

In charge
Always@VLSI Technical Club

HOD-ECE
Professor & Alternate He.
Department of ECE
K L University
VADDESWARAM
Guntur Dt., A.P., India