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Ref: KLEF/RO/ECE/CIRCULAR **Date: 15-03-2021**

CIRCULAR

Sub: Organizing event "Workshop" for the students of Electronics and Communication Engineering, of Vaddeswaram Campus of KLEF – Reg.

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This is to inform that the Department of Electronics and Communication Engineering, KLEF, is Organizing a "Workshop on VLSI Layout Design and Physical Design Automation" for the students of Electronics and communication Engineering, Vaddeswaram Campus of KLEF on, 18-03-2021, as details below:

Event Name: "Workshop"
Date: 18-03-2021
Venue: R-106

All the students of ECE, are invited to attend this program.
Dy-HOD's & Year coordinators are requested to bring this information to the attention of all ECE students and encourage them to participate in this program.

HOD-ECE
Professor & Alternate HOD
Department of ECE
K L University
VADDESWARAM
Guntur Dt., A.P., India

To
All ECE Students,
All ECE Faculty,
Principal.

Koneru Lakshmaiah Education Foundation
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Expert talk On "VLSI Layout Design and Physical Design Automation"

By

Always@VLSI

Department Of ECE

Name of the event: VLSI Layout Design and Physical Design Automation

Dates:18-03-2021

Venue:R106

No. of students participated: 52

Objective of the event:

The objective of the workshop "VLSI Layout Design and Physical Design Automation" is to provide participants with a comprehensive understanding of VLSI layout design principles and physical design automation techniques. The specific objectives include:Layout Design Fundamentals: Provide participants with a solid foundation in the fundamental principles of VLSI layout design, including layout rules, design constraints, and design-for-manufacturability considerations.Mastery of Layout Tools: Familiarize participants with industry-standard layout design tools and software, such as Cadence Virtuoso, Synopsys IC Compiler, and Mentor Graphics Calibre, enabling them to create and optimize VLSI layouts efficiently.Physical Design Automation: Introduce participants to physical design automation techniques, including floorplanning, placement, routing, and design rule checking (DRC), to automate and streamline the physical design process.

Advanced Layout Techniques: Explore advanced layout techniques, such as custom routing, clock tree synthesis, power grid design, and interconnect optimization, to improve layout quality, performance, and manufacturability.Design Rule Checking and Verification: Teach participants how to perform design rule checking (DRC) and layout versus schematic (LVS) verification to ensure the correctness and integrity of VLSI layouts, minimizing the risk of

design errors and manufacturing defects.Timing Closure and Signal Integrity: Address timing closure and signal integrity issues in VLSI layout design, including timing optimization, clock tree synthesis, signal propagation delay analysis, and noise immunity enhancement, to meet timing requirements and ensure reliable circuit operation.Yield Enhancement Techniques: Discuss yield enhancement techniques in VLSI layout design, including layout optimization for manufacturing variability, lithography-aware layout decomposition, and design for manufacturability (DFM), to improve manufacturing yield and reduce production costs.

Description of the event:

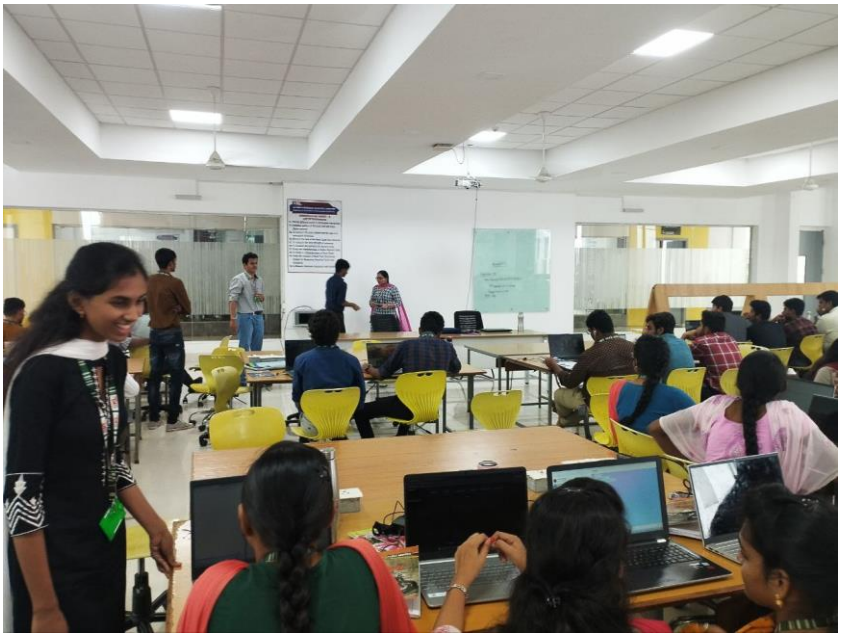
The workshop "VLSI Layout Design and Physical Design Automation" is a comprehensive program designed to equip participants with the essential skills and knowledge needed to excel in VLSI layout design and physical design automation. Over the course of the workshop, participants will delve into the intricacies of VLSI layout design, learning fundamental principles such as layout rules, design constraints, and manufacturability considerations. Through hands-on exercises and practical demonstrations, attendees will gain proficiency in industry-standard layout design tools and software, enabling them to create and optimize VLSI layouts efficiently. The workshop also covers advanced layout techniques, including custom routing, clock tree synthesis, and power grid design, empowering participants to enhance layout quality, performance, and manufacturability.

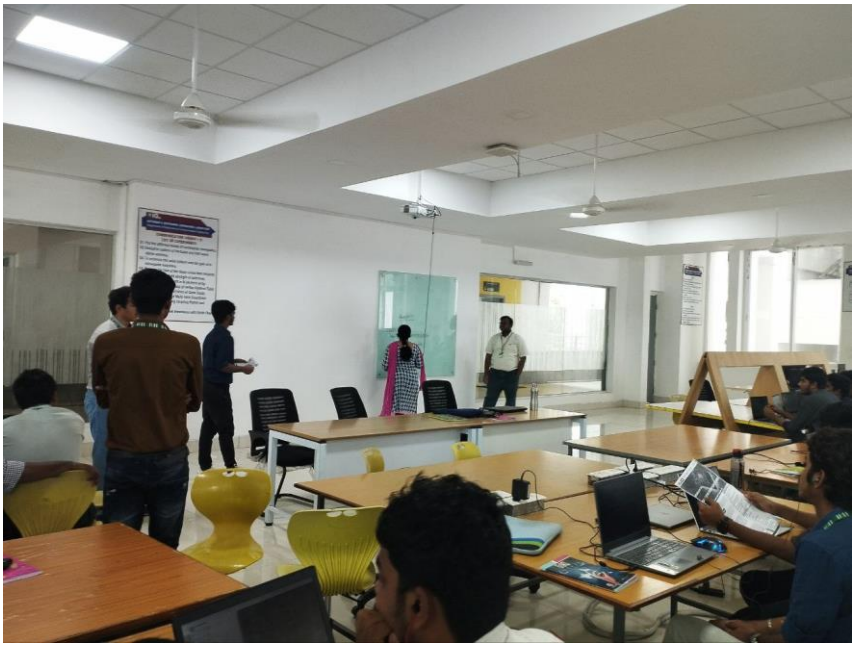
Moreover, the workshop focuses on physical design automation techniques, encompassing floorplanning, placement, routing, and design rule checking (DRC). Participants will learn how to automate and streamline the physical design process, improving design productivity and efficiency. Discussions on timing closure, signal integrity, yield enhancement, and design-for-testability (DFT) techniques will further enrich participants' understanding, enabling them to address critical aspects of VLSI layout design and ensure reliable circuit operation. Through real-world case studies and industry best practices, participants will gain practical insights into successful design implementations, preparing them to tackle complex VLSI layout design challenges with confidence and proficiency.

Outcome of the event:

The outcome of the workshop "VLSI Layout Design and Physical Design Automation" is participants who are equipped with the essential skills, knowledge, and tools necessary to excel in VLSI layout design and physical design automation. Through hands-on exercises, practical demonstrations, and discussions on advanced techniques and best practices, attendees will gain proficiency in industry-standard layout design tools, understand fundamental layout principles, and master physical design automation techniques. Armed with this expertise, participants will be able to develop high-quality VLSI layouts, optimize design productivity, enhance circuit performance, and ensure reliable operation while adhering to design rules, manufacturability constraints, and industry standards.

Photos of the event:





Students learning layout design rules.

Participant's List:

S. No	Name of the Student	Register Number	Branch	Signature
1.	180049009	KILARU SAI PRASANTH	ECE	
2.	180049008	J PAVAN PHANEENDRA MANIKUMAR	ECE	
3.	180049007	IRRINKI NAGA DURGA RAJESH	ECE	
4.	180049003	B SHIVA KUMAR	ECE	
5.	180040757	HARISH KUMAR DHARAVATH	ECE	
6.	180040743	MUDIYALA LOKESH REDDY	ECE	
7.	180040737	KADALI SAI SNEHA	ECE	
8.	180040726	MADENENI VENKAT CHANDU	ECE	
9.	180040721	MADHURI TAMMA	ECE	
10.	180040716	RANGISETTY LEELA KRISHNA	ECE	
11.	180040704	PERUMALLA GIRISH BABU	ECE	
12.	180040698	KURUGUNTLA TANUJA	ECE	
13.	180040695	KALIDINDI NAVEEN	ECE	
14.	180040692	S V SIVA KISHORE	ECE	
15.	180040679	MANNEPALLI VENKATA RAMARAJU	ECE	
16.	180040662	GADDAM VAISHNAVI	ECE	
17.	180040647	PREMITHA CHEEMAKURTHI	ECE	
18.	180040645	CHINTAPOODI PAVANKALYAN	ECE	
19.	180040641	SANAGAVARAPU SAIKUMAR	ECE	
20.	180040635	ATMAKURI KAVYA	ECE	
21.	180040604	VASIREDDY BALASARASWATHI	ECE	
22.	180040590	POLURU JEEVAN REDDY	ECE	
23.	180040585	JAMPANI YUGESH	ECE	
24.	180040582	JALDU VENKATA NAGA SASIDHAR	ECE	
25.	180040579	VADDEMPUDI SONY	ECE	
26.	180040577	D VEERA JANARDHANA ACHARI	ECE	
27.	180040576	SIDDINENI POOJA NAIDU	ECE	
28.	180040556	SHAIK LUBNA KOWSAR	ECE	

29.	180040552	NALAMASA SUSHURUTH	ECE	
30.	180040546	PAKANATI A PAVAN KUMAR	ECE	
31.	180040542	K SRI VENKATA SHANMUKHA PRIYA	ECE	
32.	180040534	GUNDAVARAM VARSHITH RAO	ECE	
33.	180049020	SHAIK THAHERUNNISA	ECE	
34.	180049014	S LOHITH NAGA SAI BRAHMENDRA	ECE	
35.	180049012	KONAKATI SAI KIRAN	ECE	
36.	180049010	KADALI JAGADEESH	ECE	
37.	170041042	ELURI DHATHRI	ECE	
38.	170041040	PARASU SAI PRASANTHI	ECE	
39.	170041039	LAKKAKULA SAI SUMA	ECE	
40.	170041037	UPASI VENKATA KRISHNA CHAITANYA	ECE	
41.	170041036	RAVURI ESWAR TEJA	ECE	
42.	170041035	PULLAMSETTI SUMAN	ECE	
43.	170041032	MANEPALLI SATYA SAI VITHAL TEJA	ECE	
44.	170041029	NIKHIL TEJA K	ECE	
45.	170041027	BANDARU AVINASH	ECE	
46.	170041024	VEERANKI JYOTHIRMAI	ECE	
47.	170041023	THORLIKONDA GOPI	ECE	
48.	170041019	RAJABOINA MANOJ MAHINISH	ECE	
49.	170041014	KOLLA NARASIMHA	ECE	
50.	170041013	KOLA RAMYA SRI VENI	ECE	
51.	170041012	KANDRU BHARATH	ECE	
52.	170041010	IDARAPALLI SAI SOURAV	ECE	

In charge
Always@VLSI Technical Club

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