Koneru Lakshmaiah Education Foundation
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Ref: KLEF/RO/ECE/CIRCULAR   **Date: 30-01-2022**

CIRCULAR

Sub: Organizing event "Workshop" for the students of Electronics and Communication Engineering, of Vaddeswaram Campus of KLEF – Reg.

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This is to inform that the Department of Electronics and Communication Engineering, KLEF, is Organizing a "Workshop on Mixed-Signal VLSI Design: Integration and Optimization" for the students of Electronics and communication Engineering, Vaddeswaram Campus of KLEF on, 02-02-2022, as details below:

Event Name: "Workshop"
Date: 02-02-2022
Venue: R-106

All the students of ECE, are invited to attend this program.
Dy-HOD's & Year coordinators are requested to bring this information to the attention of all ECE students and encourage them to participate in this program.

HOD ECE
Dr M. Suman
Dr. M. SUMAN
Professor & Head
Department of ECE
KLEF
Green Fields, Vaddeswaram
Guntur Dist., A.P. PTN 522 502

To
All ECE Students,
All ECE Faculty,
Principal.

A Two-day Workshop On "Mixed-Signal VLSI Design: Integration and Optimization".

By

Always@VLSI
Department Of ECE

Name of the event: Mixed-Signal VLSI Design: Integration and Optimization

Dates:02-02-2022

Venue:R106

No. of students participated: 49

Objective of the event:

The objective of the workshop "Mixed-Signal VLSI Design: Integration and Optimization" is to provide participants with a comprehensive understanding of mixed-signal VLSI design principles, methodologies, and optimization techniques. Specifically, the workshop aims to:Explore Mixed-Signal Design Fundamentals: Introduce participants to the fundamental principles of mixed-signal VLSI design, including analog and digital circuit integration, signal processing, and interfacing techniques. Participants will gain a solid foundation in mixed-signal design concepts, enabling them to effectively integrate analog and digital components on a single chip.Master Mixed-Signal Design Tools and Techniques: Familiarize participants with industry-standard mixed-signal design tools and software, such as Cadence Virtuoso, Synopsys Custom Compiler, and MATLAB/Simulink, as well as simulation and verification techniques specific to mixed-signal circuits. Through hands-on exercises and practical demonstrations, participants will learn how to design, simulate, and validate mixed-signal VLSI circuits effectively.

Optimize Mixed-Signal Circuit Performance: Provide participants with advanced optimization techniques for mixed-signal VLSI circuits, including noise analysis, power optimization, layout considerations, and mixed-signal co-design strategies. Participants will learn how to optimize mixed-signal circuits for performance, power efficiency, area, and manufacturability.Address Challenges in Mixed-Signal Design: Discuss common challenges and limitations encountered in mixed-signal VLSI design, such as noise, mismatch, signal integrity issues, and cross-domain interactions. Participants will learn practical strategies and solutions for overcoming these challenges, ensuring robust and reliable mixed-signal circuit designs.Foster Innovation and Collaboration: Encourage participants to explore innovative approaches and techniques in mixed-signal VLSI design, fostering creativity and collaboration within the field. Through interactive sessions, discussions, and case studies, participants will have the opportunity to exchange ideas, share experiences, and learn from each other's perspectives.

Description of the event:

The objective of the workshop "Mixed-Signal VLSI Design: Integration and Optimization" is to equip participants with a comprehensive understanding of mixed-signal VLSI design principles, methodologies, and optimization techniques. Through interactive sessions, practical demonstrations, and hands-on exercises, participants will delve into the fundamental concepts of mixed-signal design, including the integration of analog and digital circuits, signal processing, and interfacing techniques. By gaining a solid foundation in mixed-signal design fundamentals, participants will be able to effectively navigate the complexities of designing integrated circuits that combine analog and digital functionalities on a single chip.

Moreover, the workshop aims to familiarize participants with industry-standard mixed-signal design tools and software, enabling them to design, simulate, and validate mixed-signal VLSI circuits with confidence and proficiency. Participants will learn advanced optimization techniques for mixed-signal circuits, including noise analysis, power optimization, layout considerations, and mixed-signal co-design strategies. By mastering these optimization techniques, participants will be able to develop high-performance, low-power mixed-signal circuits that meet the stringent requirements of modern integrated systems. Through practical learning experiences and collaborative discussions, the workshop seeks to empower participants to address challenges in mixed-signal design effectively, fostering innovation and excellence in the field of mixed-signal VLSI design.

Outcome of the event:

The outcome of the workshop "Mixed-Signal VLSI Design: Integration and Optimization" is participants who are proficient in designing, simulating, and optimizing mixed-signal VLSI circuits with a deep understanding of integration and optimization techniques. Equipped with advanced knowledge and skills gained from interactive sessions, practical demonstrations, and hands-on exercises, participants will be able to effectively navigate the complexities of mixed-signal design, integrating analog and digital functionalities on a single chip while optimizing performance, power efficiency, area, and manufacturability. Additionally, participants will be empowered to address challenges in mixed-signal design such as noise, mismatch, signal integrity issues, and cross-domain interactions, fostering innovation and excellence in the field of mixed-signal VLSI design.

Photos of the event:

Faculty explaining the mixed signal circuit design

Students practicing the mixed signal design.

Participant's List:

S.NO	ID.NO	NAME	BRANCH	SIGNATURE
1.	2000049015	YADALA VENKATA NITHISH KUMAR	ECE	
2.	2000049012	RAMALA DHEERAJ	ECE	
3.	2000049011	KAMMILI LALITH MADHAV	ECE	
4.	2000049009	VADDI DEEPAK	ECE	
5.	2000040320	KOTLA CHENNA KESHAVA REDDY	ECE	
6.	2000040317	CHEVURI CHARAN TEJA	ECE	
7.	2000040307	CHALLAGUNDLA KAVYA	ECE	
8.	2000040304	MIRIYALA ASHOK	ECE	
9.	2000040301	PINNINTI JAYA PRAKASH	ECE	
10.	2000040298	THOTA NAGAMANI	ECE	
11.	2000040295	MATTA DEVI SREE REDDY	ECE	
12.	2000040290	GUNDUBOYINA VIJAY KUMAR	ECE	
13.	2000040281	VANTEDDU PRAVEEN REDDY	ECE	
14.	2000040273	GAYATHRI KETINENI	ECE	
15.	2000040272	APPANI GOPICHANDU	ECE	
16.	2000040270	PODURI ABHISHEK SURYA	ECE	
17.	2000040269	MANOJ KUMAR ROKKAM	ECE	
18.	2000040268	GANDREDDI CHAITANYA NAIDU	ECE	
19.	2000040258	PATHAN HASAN ZAHEERKHAN	ECE	
20.	2000040257	GURRAM SURYA KANTH SUJITH	ECE	
21.	2000040256	NALI BHARGAVA	ECE	
22.	2000040252	KOTA LAKSHMI MANOGNA	ECE	
23.	2000040249	BODDOJU VISHNU VARDHAN CHARI	ECE	
24.	2000040245	S. GURRAMPATI PREETHI REDDY	ECE	
25.	2000040244	P. VISHNU VARDHAN	ECE	
26.	2000040243	B. THANNEERU VENKANNA BABU	ECE	
27.	2000040241	GOTTUMUKKALA TARUN	ECE	
28.	2000040238	DANTHANALA SASI KANTH	ECE	

29.	2000040236	KODI RAVINDRANADH	ECE	
30.	2000040235	RAAVI PAVAN KUMAR	ECE	
31.	2000040233	ILA NAVEEN	ECE	
32.	2000040232	MOHAMMAD IBRAHIM	ECE	
33.	190040545	VANGA SATVIK REDDY	ECE	
34.	190040537	VADREVU RUTHVIK SHARMA	ECE	
35.	100040534	URLANA YASWANTH	ECE	
36.	190040525	TUMMALA RASATHVIKA	ECE	
37.	190040524	TUMMALA KARTHIK	ECE	
38.	190040522	TORATI AJAY CHANDRA	ECE	
39.	190040513	TARIGONDA JAHNAVI	ECE	
40.	190040506	SYAMALA NAGA KOTI REDDY	ECE	
41.	190040503	SUREDDY DINESH REDDY	ECE	
42.	190040501	SURAGAM GNANENDRA	ECE	
43.	190040495	SUBRAMANYAM YADAVILLI	ECE	
44.	190040483	SISTLA SATHWIC SANJAY	ECE	
45.	190040474	SHAIK MOHAMMED KHAALID	ECE	
46.	190040470	SHAIK JOHN ASIF	ECE	
47.	190040468	SHAIK GOUSE RABBANI	ECE	
48.	190040462	SHAIK ABDUL VADOOD	ECE	
49.	190040460	SHAIK HAMEED BASHA	ECE	

In charge
Always@VLSI Technical Club
Mr S. Vamsee Krishna

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