KL UNIVERISTY
FIRST SEMESTER 2010-11
Course Handout
Academic Division

Dated: 07-07-2010

Course No. : **EC C201**
Course Title : **Digital Logic Design**
Course Structure : **3-0-2**
Course coordinator : **Dr Habibulla Khan**
Instructors : **M Ravi Kumar, MV Ganesh, P. Srikanth, B.T.P. Madhav, N. Durga Indira, Naseem Shaik, Praveen.B, T.K. Sasanka**

1. Course Description:

Two level and multilevel gate implementations, simplification of logic expressions, logic families. Combination logic circuit design, Sequential logic circuit design. Flip-Flops, Shift registers, Counters, Sequence generators. PLA and PAL, State tables and State diagrams, thereshold logic.

2. Scope and Objective of the Course:

The course is designed for the second year first semester students. The course will provide an over view of the study of logic gates and their applications. The course will give an idea to simplify a given logical expression so that hardware reduction is obtained. Given a problem, the course gives the student an idea to design a logic circuit. Student get an idea about the design of various combinational and sequential logic circuits which are very useful in communications and computers. At the end of the course the student is expected to possess knowledge in designing different types of logic circuits for various applications.

3. Books:

(i) Textbook:

a. M Morris Mano, "Digital Logic and Computer Design", PHI, 2003.
b. Ronald J Tocci, "Digital Systems", Pearson Education, 9th Edition.

(ii) Reference Book:

a . Khan & Khan, "Digital Logic Design", Scitech, 2008
b. Zvi Kohavi, "Switching and Finite Automata Theory", 2nd Edition, TMH.
c. RP Jain, "Modern Digital Electronics", 3rd Edition, TMH, 2003

4. Syllabus:

UNIT – I

AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR gates, and their implementation using NAND and NOR gates, two level and multi level NAND and NOR implementations. Types of Boolean expressions, simplifications of Boolean expressions(using Boolean laws and theorems, K-maps up to four variables) Logic Families: Classification and characteristics of logic families, RTL, DTL, TTL, ECL, IIL, MOS and C-MOS logic families and their comparison.

UNIT–II

COMBINATIONAL LOGIC CIRCUITS: General design procedure for Combinational logic circuits, Design and applications of Binary Adders and Subtractors, Comparators, Encoders, Decoders, Multiplexers and De-multiplexers, Design of BCD to 7 Segment Decoder, Code converters, Sequence Generator, Parity Generator and Checker, BCD Adder / Subtractor, Carry look ahead adders, Programmable logic devices, PLA and PAL.

UNIT – III

Flip-Flops - SR, JK, D, T and Master Slave their characteristic equation, characteristic and excitation table, conversion of flip flops, Edge triggering and level triggering,

UNIT – IV

Register – Shift register – universal shift register, Asynchronous /Ripple up/Down counter, mod counters, State table and State diagrams for Flip-Flops

UNIT – V

Threshold Logic: Introduction concepts, Synthesis of Threshold functions, capabilities and limitations of threshold gate.

5.Course Plan:

Course plan is meant as a guideline. There may probably be changes.

Lec No.	Learning Objective	Topics to be covered	Reference
		UNIT - I	
1	Introduction	Implementation using NAND/NOR Gates	T1 82
2	Two level Implementation	Implementation of expressions with two level NAND/NOR gates.	T1 82-85
3	Multilevel Implementation	Implementation of expressions with two level NAND/NOR gates.	T1 85-91
4	Types of Boolean expressions simplification using Boolean laws	SOP and POS expressions minterms and maxterms Simplification of Boolean expressions.	T1 37-44
5	Simplification using DeMorgan's theorems	Simplification of Boolean expressions using DeMargan's theorems.	T1 43-44
6-9	Simplification using K-maps	Types of K-maps. Simplification using K-maps, Don't care conditions, simplification of POS expressions.	T1 64-80
10	Logic families	Classification and Characteristics of logic families.	T1 398-400
11	RTL and DTL	Circuit diagram, operation and characteristics of RTL and DTL	T1 408
12	TTL, ECL, IIL	Circuit diagram, operation and characteristics of TTL, ECL and IIL.	T1 410-420

13	MOS Logic families	Classification, circuit and characteristics of PMOS, NMOS and CMOS.	T1 421-423
14	Comparision of logic families	Comparision of various logic families.	T1 411
15	Introduction	General design procedure for CLC'S and examples of design.	T1 111-115
16	Binary adders	Half adder and full adder Design.	T1 119-122
17	Binary subtractors	Half and full subtractor Design.	T1 126-128
18	Encoders and Decoders	Design and applications of encoders and decoders.	T1 134, 139
19	DeMulriplexers and Multiplexers	Design and applications of DeMux and Mux.	T1 141
20	BCD – 7-Segment decoders	Design of BCD-7-Segment decoder	R1 4.36
21	Code converters and sequence Generators	Design of various code converters and sequence generators.	R1 6.25
22	Parity Generators and Checker	Design of odd and even parity generators and checkers.	R1 4.45
23	BCD adder/subtractor, carry look ahead adder	Design of BCD adder/subtractor and carry look ahead adder.	R1 4.53-4.58
24	PLA	What is PLA. Design procedure for PLA'S	T1 276
25	PAL	What is PAL. Design procedure for PAL	T1 280
26	SR and JK Flip-Flops	Basic SR and JK flip-flops. Design of SR and JK flip-flops. Advantages and Drawbacks.	T1 167-169
27	D and T flip-flops	Design of D and T flip-flops. Advantages and Drawbacks.	T1 169
28	Master Slave JK flip-flop	Race around condition. Design of M/S JK flip-flop.	T1 174
29	Characteristics and excitation table	Design of characteristic and excitation tables of various flip-flops.	T1 177-178
30	Conversion of flip-flops	Design procedure for convert one type of flip-flop to other type.	R1 5.23
31	Edge triggering and Level triggering	Edge triggering and Level triggering	R1 5.8
32	Register - Shift register	What is a register. Shift register. Different modes of operations.	T1 217-219
33	Applications of Shift registers, Universal Shift register	Applications of Shift registers Design and operation of universal shift register.	T1 219 225-226
34	Asynchronous counters	Asynchronous counter. Different types of Asynchronous counters	T1 227
35	Mod Counters	Mod number, Mod counter, Different types of Mod counters.	T1 239
36	Synchronous counters	Design of synchronous counters	T1 232
37	State tables	Preparation of stable tables for various flip-flops.	R1 5.29

38	State diagrams	Preparation of state diagrams for various flip-flops.	R1 5.29-5.38
39	Introduction	Threshold logic, the threshold element	R2 189-190
40	Capabilities and limitations	C & L of threshold logic	R2 193-195
41	Synthesis of threshold networks	Unate functions, Geometrical representation linear separability	R2 197-202
42-43	Identification and realization of threshold functions	Identification and realization of threshold functions	R2 202-205
44-45	Map as a tool in synthesizing threshold networks	Map as a tool in synthesizing threshold networks	R2 205-209

6.Self learning material:

Unit	Topic	Source
I	ECL, CMOS	T1
II	Design of BCD- 7- segment display	R1
	PAL	T1
III	Edge triggering	R1
IV	Universal shift register Up/down counter	T1
V	Capabilities and limitations of threshold gate	R2

7.Evaluation Scheme:

Component	Duration (minutes)	% Weightage	Marks	Date & Time	Venue
Test-1	50 Min	7.5	10	10-08-2010 9.30 to 10.20 A.M	CSE001,002, 004, 005, 101, 102,104,105, 106,201,204, 205,301,502, 509, NSH
Test-2	50 Min	7.5	10	14-09-2010 9.30 to 10.20 A.M	CSE001,002, 004, 005, 101, 102,104,105, 106,201,204, 205,301,502, 509, NSH
Assignment submission		3.75	5	Continuous	
Assignment Test	50 Min	3.75	5	26-10-2010 9.00 to 10.20 A.M	CSE001,002, 004, 005, 101, 102,104,105, 106,201,204, 205,301,502, 509, NSH
Quiz	30 Min	3.75	5	26-10-2010 9.00 to 10.20 A.M	CSE001,002, 004, 005, 101, 102,104,105, 106,201,204, 205,301,502, 509, NSH
Regular Lab Evaluation	Continuous	12.5	50		
Comprehensive Lab Exam	3 Hrs	10	40		
Comprehensive Exam	3 Hrs	45	60		
Attendance for Theory & Tutorial		3.75	5	Continuous	
Attendance for Lab		2.5	10	Continuous	

8. Chamber consultation hour: Informed in the class in first week.

9. Notices: All notices regarding the course will be put in E-learning website.

Course Coordinator