

KL UNIVERISTY
FIRST SEMESTER 2010-11
Course Handout
Academic Division

Dated: 07-07-2010

Course No. : EM C205
Course Title : Computer Organization
Course Structure : 3-0-0
Course coordinator : Manoj Kumar Tyagi
Instructors : M.Venkatewara Rao

1. Course Description:

This course provides basic Knowledge necessary to understand the hardware operation of digital computers and covers the three subjects associated with computer hardware. It describes Physical organization of a particular computer including its registers,dataflow,Micro operations and control Function by means of a hardware description language.

2. Scope and Objective of the Course:

This subject deals with computer architecture as well as computer organization and design. computer architecture is concerned with the structure and behaviour of the various functional modules of the computer and how they interact to provide processing needs of the user. computer organization is concerned with the way the hardware the components are connected together to form a computer system. computer design is concerned with the development of the hardware for the computer taking in to consideration a given set of specification.

3. Books:

(i) Textbook:

- a. 1.Morris M.Mano,"Computer Systems Arichitecture",3rd Edition, Prentice Hall of India, New Delhi, 1993.

(ii) Reference Book:

- a. John P Hayes," Computer Arichitecture and Organization", 3rd Edition,Mc- Graw Hill,1997,New York,N.Y.,U.S.A.
- b. V.Carl Hamacher et.al,"Computer Organization" 5th Edition,Mc-GrawHill,New York,2001,N.Y.,U.S.A.
- c. Raja Raman and Radha Krishna," Computer architecture and organization"-PHI,2006,New Delhi

4. Syllabus:

UNIT I:

REGISTER TRANSFER & MICRO-OPERATIONS: Register Transfer Language, Register Transfer, Bus&memory Transfers, Arthmetic Micro-operations, Logic Micro Operations, Shift Micro-operation, Arithmetic Logic Shift Unit.

UNIT II:

BASIC COMPUTER ORGANISATION AND DESIGN: introduction codes, Computer Registers, Computer instructions, Timing and Control, Instruction Cycle, Memory-Reference Instruction, Input-Output and interrupt, Design of Basic Computer, Design of accumulator

Logic, **MICRO PROGRAMMED CONTROL:** Control Memory, Address Sequencing, Micro-Program example, Design of Control Unit.

UNIT III:

CENTRAL PROCESSING UNIT: General registers Organization, Stack Organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation,

Program Control, Reduced instruction Set Computer (RISC). **COMPUTER ARITHMETIC:** Addition and Subtraction, Multiplication Algorithms, Division Algorithms Floating-point Arithmetic Operations.

UNIT IV:

MEMORY ORGANIZATION: Memory Hierachy, Main Memory, Auxiliary memory, Associative Men Cache Memory, Virtual Memory, Memory Management hardware.

UNIT V:

INPUT-OUTPUT ORGANISATION: Peripheral Devices, input-Output interface, Asynchronous Data Tranfer, Modes of Transfer, Priority interrupt, Direct Memory Access (DMA), input –output Processor, serial Communication

5.Course Plan:

Course plan is meant as a guideline. There may probably be changes.

Lecture No.	Learning Objectives	Topics to be covered	References
1	Register transfer language	Register transfer language	T1 p. 93
2	Register transfer	. Register transfer, Control Transfer.	T1 p.95
3	Bus and memory transfers	Three state Bus Buffers, Memory transfer	T1 p.97
4	Arithmetic micro operations	Binary Adder, Binary Adder-Subtractor, Binary incrementer, Arithmetic Circuit.	T1 p.102
5	Logic micro operations	List of Logic micro operations. Hardware Implementation ,Some applications	T1 p.108
6	Shift micro operations	Hardware Implementation	T1 p.114
7	Arithmetic Logic Shift Unit	Arithmetic Logic Shift Unit	T1 p.116
8	Instruction codes	Stored program Organization, Indirect Address	T1 p.125
9	Computer Registers, Computer Instructions	Common Bus System, Instruction set completeness	T1 p.129-136
10	Timing & Control, Instruction cycle	Fetch & Decode, determine the type of Instruction, Register Reference Instruction	T1 p.137-145

11	Memory reference Instruction	AND to AC,ADD to AC, LDA:Load to AC,STA,BUN,BSA,ISZ.	T1 P147
12	Input-Output and Interrupt	I/O Configuration,I/O Instructions,Program Interrupt,Interrupt cycle.	T1 p.152
13	Design of Basic Computer	Control Logic gates,control of registers and memory,control of single fipflop,control of common bus.	T1 p.159
14	Design of accumulator logic	Control of AC register,adder and logic circuit	T1 p.166
15	Control Memory	Control Memory	T1 p.215
16	Addressing Sequencing	Conditional Branching,mapping of instructions,sub Routines	T1 p.218
17	Micro Program Example	Computer configuration,Micro instruction format,Symbolic micro instruction,the fetch routine,binary micri program	T1p.222
18	Design of Control Unit	Micro program Sequencer.	T1 p.233
19	General Register Organization	Control Word,Examples of micro operations	T1 p.244
20	Stack Organization	Register stack,memory stack,reverse polish notation,Evaluation of arithmetic expression.	T1 p.249
21	Instruction Format	Three- address,two address,one address,zero address RISC instructions.	T1 p.257
22	Addressing Modes	Immediate ,Register,Register indirect,implied,Auto Increment&decrement,direct,indirect,r relative,indexed addressing modes	T1 p.262
23	Data Transfer manipulation	Data Trasfer&Manipulation instructions arithmetic instruction logical and bit manipulation instruction	T1 p.268
24	Program Control	Status bit conditions,conditional branch instructions subroutine call and return,program interrupt,types of interrupts.	T1 p.275
25	Reduced Instruction Set Computer(RISC)	CISC Characterstics,Risc Characterstics	T1 p.284
26	Arithmetic addition &Subtraction Algorithm	Additional Subraction with signed magnitude data&with signed two,s complement data,Hardware implementation.	T1 P.336
27	Multiplication Algorithms	Signed Magnitude data,Hardware implementation,booth Multiplication algorithm,arry multiplier.	T1 p.342
28	Division Algorithms	Hardware implementation for signed magnitude data,Devide overflow,Hardware algorithm	T1 p.350

29	Floating Point Arithmetic Operation	Basic Conditions, Register configuration, addition and subtraction.	T1 p.356
30	Floating Point Arithmetic Operation	Multiplication & division	T1 p.356
31	Memory hierarchy	Auxiliary Memory, cache memory, multiprogramming,	T1 p.445
32	Main Memory	RAM and ROM Chips, Memory Address Map, Memory connection CPU.	T1 p.448
33	Auxiliary Memory	Magnetic disk, Magnetic tape	T1 p.454
34	Associative and cache Memory	Associative Mapping, direct, set-Associative Mapping, writing into cache, cache initialization	T1 p.458-471
35	Virtual Memory	Address space and Memory Space Address mapping using pages, page Replacement	T1 p.471
36	Memory Management Hardware	Segmented page Mapping, Memory Protection	T1 p.478
37	Peripheral Devices	Peripheral. Monitor and keyboard, printer, Magnetic tape, Magnetic Disk.	T1 p.383
38	Input-Output Interface	I/O Bus and interface Module, I/O versus memory buses, isolated versus Memory mapped I/O.	T1 p.387
39	Asynchronous data transfer	Strobe control, Hand shaking. Asynchronous serial transfer, Asynchronous communication interface, FIFO Buffer.	T1 p.393
40	Modes of Transfer	Programmed I/O, Interrupt initiated I/O	T1 p.402
41	Priority Interrupt	Daisy chaining priority, parallel priority interrupt, Priority encoder, interrupt cycle.	T1 p.409
42	Direct Memory Access	DMA Controller, DMA Transfer	T1 p.417
43	Input-Output Processor	CPU-IOP Communication	T1 p.422
44	Input-Output Processor	Intel 8089 IOP	T1 p.422
45	Serial Communication	Character oriented protocol, Data Transparency, Bit oriented Protocol	T1 p.431

6. Self learning material:

Unit	Topic	Source
I	Binary adder subtractor	Morris M.Mano,"Computer Systems Architecture",3 rd Edition
II	Adder and logic circuit	Morris M.Mano," Computer Systems Architecture",3 rd Edition.
III	Data manipulation instructions	V.Carl Hamacher et.al,"Computer Organization"2 nd Edition
V	RISC	Computer Organization by William Stallings
V	Numerical Example	Morris M.Mano," Computer Systems Architecture",3 rd Edition
V	CPU-IOP communication	Computer architecture and organization by Raja Raman and Radha Krishna-PHI

7.Evaluation Scheme:

Component	Duration (minutes)	% Weightage	Marks	Date & Time	Venue
Test-1	50 Min	10	10	11-08-2010 9.20 to 10.20 A.M	CSE103,202, 209,309
Test-2	50 Min	10	10	15-09-2010 9.20 to 10.20 A.M	CSE103,202, 209,309
Assignment submission		5	5		
Assignment Test	50 Min	5	5	27-10-2010 9.00 to 10.20 A.M	CSE103,202, 209,309
Quiz	30 Min	5	5	27-10-2010 9.00 to 10.20 A.M	CSE103,202, 209,309
Regular Lab Evaluation	Continuous	0	0		
Comprehensive Lab Exam	3 Hrs	0	0		
Comprehensive Exam	3 Hrs	60	60		
Attendance for Theory & Tutorial		5	5	Continuous	
Attendance for Lab		0	0	Continuous	

8. Chamber consultation hour: Informed in the class in first week.

9. Notices: All notices regarding the course will be put in E-learning website

Course Coordinator