13-EC555 LOW POWER VLSI CIRCUITS

SYLLABUS

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. **Device & Technology Impact on Low Power:** Dynamic dissipation in CMOS, Transistor sizing& gate oxide thickness, Impact of technology Scaling, Technology & Device innovation. **Simulation Power analysis**: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation. **Probabilistic power analysis**: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. **Low Power Circuit's**: Transistor and gate sizing, network restructuring and Reorganization. Special Flip Flops & Latches design, high capacitance nodes, low power digital cells library. **Logic level:** Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Architecture & Systems:** Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components. **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network. **Special Techniques**: Power Reduction in Clock networks, CMOS Floating Node, Low Power Bus Delay balancing, and Low Power Techniques for SRAM.

TEXT BOOKS

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002
2. Rabaey, Pedram, "Low Power Design Methodologies" Kluwer Academic

REFERENCES

1. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000
2. Yeo, "CMOS/BiCMOS ULSI Low Voltage Low Power" Pearson Education