13-EC561 OPTIMIZATION TECHNIQUES AND APPLICATIONS IN VLSI DESIGN

**SYLLABUS**

**Statistical Modeling**: Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgroms model, principal component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models Statistical Performance, Power And Yield Analysis Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation Convex Optimization Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Max-monomial fitting, Polynomial fitting. Genetic Algorithm Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation-partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multiday Partitioning Hybrid genetic-encoding-local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm. Ga Routing Procedures And Power Estimation Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures. Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding-fitness function-GA vs Conventional algorithm.

**REFERENCES**

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3.Stephen Boyd, Lieven Vandenberghe “Convex Optimization”, Cambridge University Press,