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Industrial Talk on Physical verification Flow for DRC and LVS

Date: 27/02/2021

Department Name : **ECE**

Event Date(s) : **27/02/2021**

Event Time : **10.30am.**

Event Name : **Industrial Talk on Physical verification Flow for DRC and LVS**

Event Category : **Department Association Bodies**

Event Objective : The objective of the event on Physical Verification Flow for DRC (Design Rule Checking) and LVS (Layout vs. Schematic) is to provide attendees with comprehensive knowledge and practical insights into the physical verification process of integrated circuit (IC) designs. The event will cover the basic principles, methodologies, and industry standards related to DRC and LVS, ensuring attendees have a solid understanding of these essential aspects of IC design verification.

Resource Person : **Mr. A. Poorna Chandra Reddy, R&D Engineer, Synopsys Pvt.Ltd. Hyderabad.**

Event Venue / Room No. : **Online**

Faculty Coordinator EMP.ID : **5155**

Faculty Coordinator Name : **Dr.B.Balaji Associate Professor, ECE**

Faculty Coordinator Email-ID: balaji@kluniversity.in

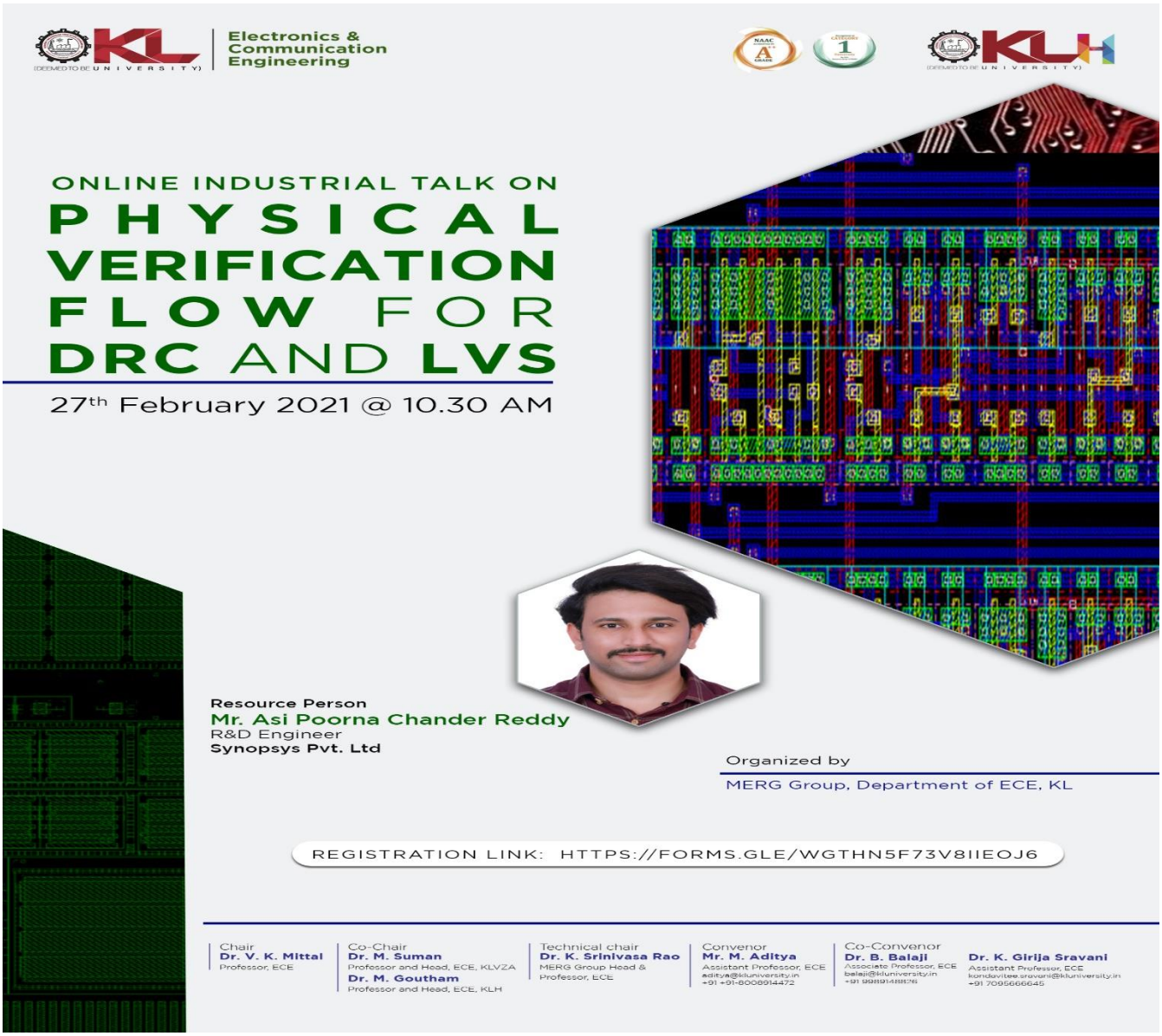
The following KLEF students have attended

No. of Volunteers Participated: 41

No. of faculty Participated: 02

S.No	Reg.No	Name of the Student
1	190040377	P AKHIL REDDY
2	190040410	PONNADI RAJENDRA
3	190040411	POTHANI PRABHUKIRAN
4	190040415	PARASARAM SUSEEL KOUSIC
5	190040438	REVU CHANIKYA RAJU
6	190040449	SAMIRAJU SAI BHANUTEJA
7	190040460	SHAIK HAMEED BASHA
8	190040468	SHAIK GOUSE RABBANI
9	2100040021	GOGINENI RUTHVIK
10	2100040022	MACHERLA DURGA SAI DEEPAK
11	2100040023	MALLINENI SREE THULASI
12	2100040024	MOKKARALA HARI GOVINDA SUBHANG
13	2100040117	RAYAPUDI NAGA SAI
14	2100040118	NADIMINTI SAI MANOJ
15	2100040119	NAKKALA ADAM RAJ
16	190040089	CHIKKARAJU ARUN
17	190040104	DANDA SAI VIJAY
18	190040108	DARLANKA NAGA VENKATA VASANTH
19	190040111	SAI SATYA SIVA VAMSI KRISHNA DASARI
20	190040117	DEVARAPALLI PAVAN CHARITH
21	190040125	DONTHI REDDY GNANA PRAKASH REDDY
22	190040140	GAVINI RUPA RANI
23	190040144	GOGINENI VASUDEV
24	190040153	GORRE VENKATA HARI PRASAD
25	190040156	GOURIPEDDI PAVANI SOWMYA
26	190040173	GURRAM RISHITHA
27	190040187	JASHTI GOPI NATH
28	190040194	KALAPALA THANUSHA
29	190040201	KANAKALA SATYA VENKATA AKASH
30	190040204	KANKANALA SAI ANURAG
31	190040216	KARUMURI DHANESH
32	190040221	KATRAGADDA SATYAKEERTHANA
33	190040231	KILARU PAVAN SAI
34	190040585	YELLAPRAGADA SRI VENU KAMAL
35	190040591	YERUVA NITESH KUMAR REDDY
36	190049024	GANAPAVARAPU VEDAVYAS

37	190049025	RAVURI ANUSHA
38	190049029	JANGALA GOPI
39	190049032	KONA JAYA SANKAR KRISHNA
40	190049034	JAMMULA SURENDRA BABU
41	190049035	SWARNA MALATHI SREE



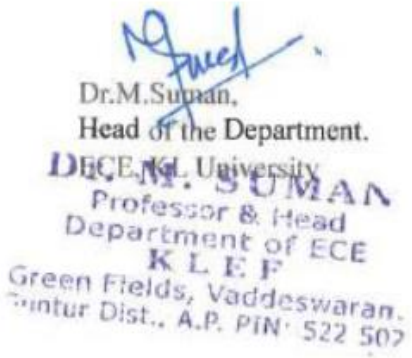
Description: The workshop on Physical Verification Flow for DRC (Design Rule Checking) and LVS (Layout vs. Schematic) offers participants an in-depth exploration of the critical processes involved in ensuring the integrity and reliability of integrated circuit (IC) designs. Designed for IC designers, verification engineers, and professionals in the semiconductor industry, this workshop provides practical insights and hands-on experience in implementing robust physical verification flows. Participants will gain a comprehensive understanding of the fundamental principles underlying DRC and LVS checks. Through interactive sessions and expert-led presentations, attendees will learn about design rule constraints, layout guidelines, and schematic consistency verification. The workshop delves into advanced techniques and methodologies for performing thorough DRC and LVS checks. Topics include handling complex design rules, managing multi-layer layouts, and addressing issues related to process variations and parasitic extraction. Participants will have the opportunity to gain practical experience by working with industry-standard physical verification tools. Through guided tutorials and interactive exercises, attendees will learn how to set up and execute DRC and LVS checks, interpret verification results, and troubleshoot common issues. The workshop provides insights into best practices and optimization strategies for improving the efficiency and accuracy of physical verification flows. Attendees will learn how to optimize rule decks, enhance layout quality, and streamline verification processes to minimize design iterations and accelerate time-to-market.

Event Outcome:

The workshop on Physical Verification Flow for DRC and LVS was highly successful in empowering participants with essential skills, knowledge, and practical insights for mastering physical verification processes in IC design. By equipping attendees with the tools and expertise needed to ensure the manufacturability and reliability of IC designs, the workshop has made a significant contribution to advancing the capabilities of semiconductor professionals and promoting excellence in integrated circuit design.

Dr.B.Balaji

Signature of Faculty Coordinator



Online Industrial Talk on "Physical verification Flow for DRC and LVS" by Micro Electronics Research Group, Department of ECE, KLEF – Reg.

Registrar <registrar@kluniversity.in>

Fri 2/26/2021 11:21 AM

To: PRESIDENT <president@kluniversity.in>; Havish <havish@kluniversity.in>; Raja H Koneru <krh@kluniversity.in>; Dr. S S Mantha <ssmantha@kluniversity.in>; Dr.Venkat <drvenkat@kluniversity.in>; Vice Chancellor - KLU <vc@kluniversity.in>; N Venkat Ram <venkatram@kluniversity.in>; Sreenivasulu <nikhi_bt@kluniversity.in>; Dr. B.Jayakumar Singh <jksingh@kluniversity.in>; Dr. Burra V L S Prasad <pburra@kluniversity.in>; Vemuri Praveen Kumar <vemuripraveen@kluniversity.in>; sudhamani <sudhamani@kluniversity.in>; Mahi <drmahi_bt@kluniversity.in>; Giridhar Kanuri <giridharkanuri@kluniversity.in>; Dr Karthikeyan S <karthikeyan@kluniversity.in>; Nadeem Siddiqui <siddiqui@kluniversity.in>; Dr ARUN C <carun@kluniversity.in>; Dr Ashish Runthala <ashish@kluniversity.in>; 1318 <felicebt@kluniversity.in>; M.Maheswara Reddy <mahesh_bt@kluniversity.in>

1 attachments (2 MB)

ECE Industrial Talk_ Poster.jpg;

Ref: KLEF/RO/HOD-ECE/2020-21 Date: 26-02-2021

Orders of the Vice-Chancellor dt.26-02-2021

CIRCULAR

Sub: Online Industrial Talk on **"Physical verification Flow for DRC and LVS"** by Micro Electronics Research Group, Department of ECE, KLEF – Reg.

Ref: Letter dated 26.02.2021 from Dr.K. Srinivasa Rao, Professor,ECE and Head-MERG forwarded by Dr.M. Suman, HoD-ECE.

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This is to inform that Micro Electronics Research Group, Department of ECE, KLEF, is conducting an online Industrial Talk on **"Physical verification Flow for DRC and LVS"** for all the students, faculty members and research scholars as per the details given below.

Speaker : **Mr. A. Poorna Chandra Reddy, R&D Engineer, Synopsys Pvt.Ltd., Hyderabad.**
Date and Time : **27.02.2021 (Saturday) at 10.30 a.m.**

Program Convener : Mr.M. Aditya,Asst. Professor, Department of ECE
Program Co Conveners**:** Dr.B. Balaji & Dr.K. Girija Sravani, Dept.of ECE, KLEF
Department Chair : Dr. V. K. Mittal, Professor, ECE
Program Chair : Dr. M. Suman, Professor & HOD, ECE
Technical Chair : Dr. K. Srinivasa Rao, Professor & Research Group Head, ECE

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Thanks & Regards

Prof. Y. V. S. S. S. V. Prasada Rao
Ph.D(Mech. Engg.)., DPM., MBA (Fin & HR)., FICWA
REGISTRAR
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