REPORT ON VISITING PROFESSOR ASSIGNMENT - ITALY

Academic Teaching, Seminar and Research Collaboration at Università degli Studi di Roma "Tor Vergata", Italy

Name	**Dr. Aravindhan Alagarsamy** Associate Professor - ECE
Affiliation	KL University, Andhra Pradesh, India
Host Institution	Università degli Studi di Roma "Tor Vergata", Italy
Department	Department of Electronic Engineering
Position	Visiting Professor
Actual Duration of Activity Completion	01 April 2026 – 30 May 2026
Maximum Duration of Activity Completion	01 April 2026 – 30 May 2026
Purpose of Visit	Teaching, specialized seminar, faculty/student engagement and research collaboration in VLSI Design, SoC/MPSoC and Network-on-Chip (NoC)

1. Objectives of the Visit

The Visiting Professor assignment at the Department of Electronic Engineering, Università degli Studi di Roma "Tor Vergata", was undertaken to contribute to teaching and research activities in the areas of VLSI Design and Systems. The assignment provided an opportunity for academic knowledge transfer, interaction with Master's students and doctoral scholars, and strengthening of international academic and research collaboration.

The specific objectives were to deliver academic lectures in VLSI Design and Systems; conduct a specialized seminar on Network-on-Chip (NoC); engage with faculty and students for academic collaboration; and contribute to research discussions related to System-on-Chip (SoC) and Multi-Processor System-on-Chip (MPSoC) architectures.

2. Academic Engagement and Orientation

The Visiting Professor engaged with the Department of Electronic Engineering and participated in scheduled teaching and academic activities during the assignment period. The activities were organized around Master's-level teaching in VLSI design and systems, together with a doctoral-level seminar on multi-processor system performance and the transition from SoC to NoC.

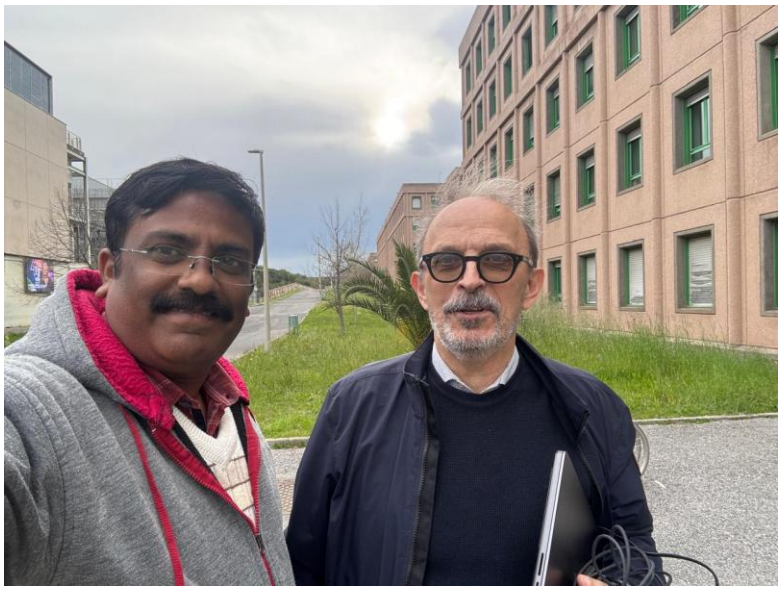

Figure 1 Academic interaction with the host faculty at Università degli Studi di Roma "Tor Vergata"

3. Teaching / Academic Activities – 20 Hours

A total of 20 hours of teaching was delivered for the Master's Degree programme in Electronics Engineering under the course "Progetto di Circuiti e Sistemi VLSI". The teaching covered the following major themes:

3.1 Static Timing Analysis (STA)

- Diversified paths existence in digital circuits.
- Delay parameters of combinational circuits.
- Delay parameters of sequential circuits.
- STA for pipeline circuits involving combinational and sequential circuits.
- STA of pipeline circuits with clock skew, including positive and negative clock skew.
- STA for pipeline circuits with clock jitter.
- STA for pipeline circuits with On-Chip Variation (OCV) and Clock Re-convergence Pessimism Removal (CRPR), including setup and hold checks.

3.2 VLSI Physical Design Automation

- Introduction to VLSI physical design.
- Partitioning and its algorithms, including the Kernighan–Lin (KL) algorithm.
- Floor planning, placement and routing – objectives, requirements and algorithms.

3.3 System-on-Chip (SoC)

- Introduction to System-on-Chip.
- SoC design flow.
- Categorization of SoC approaches.
- Multi-Processor System-on-Chip (MPSoC) concepts.

3.4 Networks-on-Chip (NoC)

- New paradigm shift and state of the art in NoC.
- Open problems for research and project development.

Figure 2 Interaction with students during the academic teaching activities

3.5 Teaching Schedule for Master's Degree Programme

Date	Day	Duration	Room	Topics Discussed
13-Apr-26	Mon	14:00–15:30	C 4	Diversified paths existence in digital circuit and delay parameters for combinational circuits (case study)
15-Apr-26	Wed	16:00–17:30	B 14	Delay parameters of sequential circuit and STA using positive/negative clock skew (setup & hold) – case study
16-Apr-26	Thu	11:30–13:00	C 12	STA using clock jitter – positive & negative (setup & hold) – case study
20-Apr-26	Mon	14:00–15:30	C 4	STA using OCV with clock reconvergence and pessimism removal (CRPR) (setup & hold) – case study
22-Apr-26	Wed	16:00–17:30	B 14	VLSI physical design automation flow – partitioning algorithm (KL algorithm) – sample problem solving
23-Apr-26	Thu	11:30–13:00	C 12	Floor planning – objective & floorplan sizing algorithm; linear ordering algorithm – sample problem solving
27-Apr-26	Mon	14:00–15:30	C 4	Placement – objective & classification of placement cells – wirelength estimation methods
29-Apr-26	Wed	16:00–17:30	B 14	Routing – terminologies & shortest routing algorithm – sample problem solving
30-Apr-26	Thu	11:30–13:00	C 12	SoC design flow – categorization of SoC approach – MPSoC concepts
04-May-26	Mon	14:00–15:30	C 4	NoC – new paradigm shift, state of the art, and open problems for research/project
Total Teaching Sessions				**20 Hours**

4. Seminar / Workshop Activities – 04 Hours

A specialized seminar titled “Multi-Processor System Performance Characteristics: From System-on-Chip (SoC) to Network-on-Chip (NoC)” was conducted for Doctorate Scholars in Electronics Engineering. The seminar was held on 13 May 2026 at 14:30 hours in Room R3, Department of Electronics Engineering.

4.1 Objective

- Evolution of multi-processor systems.
- On-chip communication architectures.
- Transition from System-on-Chip (SoC) to Network-on-Chip (NoC).
- Performance challenges and research directions in NoC designs.

4.2 Overview

The seminar provided doctoral scholars with an overview of modern multi-processor architectures and their evolution toward scalable on-chip communication paradigms. The discussion covered fundamental concepts of multi-processor systems, communication architectures and on-chip interconnection techniques, followed by the limitations of traditional SoC designs and the emergence of NoC as a scalable alternative.

Particular emphasis was placed on performance metrics such as latency, bandwidth, power consumption and scalability, together with VLSI CAD challenges including application mapping, routing, buffer sizing and simulation. The seminar also highlighted current research challenges and open problems in NoC design, enabling participants to identify potential research directions in VLSI systems, embedded architectures and high-performance computing.

Figure 3 Seminar on "Multi-Processor System Performance Characteristics: From SoC to NoC"

5. Faculty, Student and Research Interaction

The assignment facilitated direct interaction with faculty members and students of the Department of Electronic Engineering. These interactions supported academic knowledge exchange in VLSI design, SoC/MPSoC architectures and NoC systems, while also providing opportunities to discuss research directions and future collaborative activities.

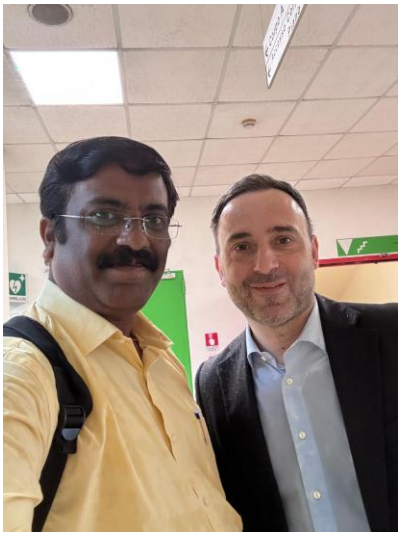

Figure 4 Interaction with a faculty member of the Department of Electronic Engineering

Figure 5 Interaction with students and academic participants during the Visiting Professor assignment

6. Future Work & Collaboration Plan

6.1 Joint Research Funding Initiatives

- Plan to submit collaborative proposals under Department of Science and Technology (DST), India, particularly Indo–EU research calls tentatively expected in October 2026.
- Explore funding opportunities through Anusandhan National Research Foundation (ANRF), India, and relevant European Union research programmes.

6.2 Scholars & Faculty Exchange Programme

- Establish a bilateral exchange programme between KL University, India, and Università degli Studi di Roma “Tor Vergata”.
- Facilitate short-term visits, joint supervision of Ph.D. scholars and collaborative research stays.

6.3 International Workshops & Academic Events

- Organize an international workshop in hybrid mode focusing on emerging research areas such as VLSI, NoC and embedded systems.
- Invite international experts, industry professionals and academic researchers for knowledge exchange.

6.4 International Symposium & Conference Proposals

- Jointly apply for organizing international symposiums with funding support from ANRF, DST and EU agencies.
- Develop platforms for presenting collaborative research outcomes.

6.5 Joint Publications & Research Output

- Promote co-authored publications in high-impact journals and conferences.
- Encourage collaborative research in interdisciplinary domains.

6.6 Industry Collaboration & Technology Transfer

- Engage with semiconductor and embedded-system industries in India and Europe.
- Promote applied research, internships and technology-transfer opportunities.

7. Key Outcomes of the Visit

- Successful completion of the assigned teaching load of 20 hours and the 4-hour specialized seminar.
- Strengthening of academic ties between Università degli Studi di Roma “Tor Vergata” and KL University, India.
- Knowledge transfer in VLSI design methodologies and Network-on-Chip systems.
- Academic interaction with Master's students and doctoral scholars.
- Identification of opportunities for joint research funding, scholar/faculty exchange, international workshops, publications and industry collaboration.

8. Compliance with Contract

As required under the Visiting Professor assignment, this report is submitted for certification of completion of duties. The assigned responsibilities were fulfilled through the completion of 20 hours of teaching and 4 hours of seminar activity, conduct of academic activities as per the agreement, and contribution to the departmental academic environment.

9. Acknowledgment

I express my sincere gratitude to the Rector, Università degli Studi di Roma “Tor Vergata”, the Department of Electronic Engineering, faculty members, students and all coordinators for their support, cooperation and warm hospitality during the Visiting Professor assignment.

10. Closure Note

The Visiting Professorship at Università degli Studi di Roma “Tor Vergata” was a highly enriching academic experience. It enabled meaningful knowledge exchange, strengthened international academic and research collaboration, and contributed to advanced learning and research engagement in VLSI, SoC/MPSoC and NoC domains.

Submitted by:

Dr. Aravindhan Alagarsamy
Associate Professor - ECE