STUDENT HAND BOOK

ACADEMIC YEAR 2018-19

MASTER OF TECHNOLOGY
VLSI

Koneru Lakshmaiah Education Foundation
(Deemed to be University estd. u/s. 3 of the UGC Act, 1956)
Accredited by **NAAC** as '**A**' Grade University ❖Approved by AICTE ❖ ISO 9001-2015 Certified
Campus: Green Fields, Vaddeswaram - 522 502, Guntur District, Andhra Pradesh, INDIA.
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Mission statement of K L E F:

Vision:

To be a globally renowned university.

Mission

To impart quality higher education and to undertake research and extension with emphasis on application and innovation that cater to the emerging societal needs through all-round development of students of all sections enabling them to be globally competitive and socially responsible citizens with intrinsic values.

Vision and Mission statement of ECE department

VISION

To evolve into a globally recognized department in the frontier areas of Electronics & Communication Engineering (ECE).

MISSION

M1- To produce graduates having professional excellence.
M2- To carry out quality research having social & industrial relevance.
M3- To provide technical support to budding entrepreneurs and existing Industries**.**

PROGRAM EDUCATIONAL OBJECTIVES (PEOS):

- **PEO1:** To mould the students to become effective global science students in the competitive environment of modern society
- **PEO2:** To provide students with strong foundation in contemporary practices of Science, different functional areas and scientific environment.
- **PEO3:** To emphasize on application oriented learning.
- **PEO4:** To develop communication, analytical, decision-making, motivational, leadership, problem solving and human relations skills of the students.
- **PEO5:** To inculcate professional and ethical attitude in students.
- **PEO6:** To pursue lifelong learning as a means of enhancing knowledge and skills necessary to contribute to the betterment of profession.

Programe Outcomes

PO Number	Description
PO1	Apply the knowledge of science, mathematics, and engineering principles for developing problem solving attitude and get sound knowledge in the theory, principles and applications of VLSI Circuits and Systems.
PO2	Configure recent EDA tools, apply test conditions, deploy and manage them.
PO3	Design and conduct experiments, analyze and interpret data, imbibe programming skills for development of simulation experiments.
PO4	Ability to demonstrate the knowledge of engineering solutions, and function as a member of a multidisciplinary team with sense of ethics, integrity and social responsibility.
PO5	To develop, design and implement projects with given specifications, in order to cater industrial needs.
PO6	Ability to investigate develops and carries out research to solve industrial problems related to designing and testing of VLSI systems.
PO7	Design a system, component or process as per social needs and specifications and also will be aware of contemporary issues.

M.TECH – VLSI COURSE STRUCTURE

First Year (First Semester):

S. No.	Course Code	Course Title	Periods			Credits
			L	T	P	
1	18 EC 5128	MOS Circuit Design	3	1	2	5
2	18 EC 5129	Algorithm for VLSI Design Automation	3	1	0	4
3	18 EC 5130	HDL & PLD Architectures	3	1	2	5
4	18 EC 5131	IC Fabrication Technology	3	1	0	4
5		Elective – 1	3	0	0	3
6		Elective - 2	3	0	0	3
7	18 IE 5149	Seminar	0	0	4	2
		Total	**18**	**4**	**8**	**26**

First Year (Second Semester) :

S. No.	Course Code	Course Title	Periods			Credits
			L	T	P	
1	18 EC 5232	Advanced Analog IC Design	3	1	2	5
2	18 EC 5233	Low Power VLSI Circuits	3	0	2	4
3	18 EC 5234	VLSI System Design	3	1	0	4
4	18 EC 5235	Testing of VLSI Circuits	3	1	0	4
5		Elective – 3	3	0	0	3
6		Elective - 4	3	0	0	3
7	18 IE 5250	Term Paper	0	0	4	2
		Total	**18**	**3**	**8**	**25**

Second Year (First & Second Semester) :

S.No	Course code	Course Title	Periods			Credits
			L	T	P	
1	18 IE 6050	Dissertation	0	0	72	36

ELECTIVE COURSES

S.No	Course code	Course Title	Periods			Credits
			L	T	P	
Elective-1						
1	18 EC 51Q1	Embedded System Design	3	0	0	3
2	18 EC 51Q2	VLSI Signal Processing	3	0	0	3
3	18 EC 51Q3	CMOS Mixed Signal Circuits	3	0	0	3
4	18 EC 51Q4	Nano Electronics	3	0	0	3
5	18 EC 51Q5	CAD Tools for VLSI	3	0	0	3
Elective-2						
1	18 EC 51R1	Image and Video Processing	3	0	0	3
2	18 EC 51R2	Bi-CMOS Technology & Applications	3	0	0	3
3	18 EC 51R3	Semiconductor Device Modeling	3	0	0	3
4	18 EC 51R4	Memory Design and Testing	3	0	0	3
5	18 EC 51R5	Reconfigurable Computing	3	0	0	3
Elective-3						
1	18 EC 52S1	System on Chip Design	3	0	0	3
2	18 EC 52S2	Process and Device Characterization Measurements	3	0	0	3
3	18 EC 52S3	Advanced VLSI Design	3	0	0	3
4	18 EC 52S4	MEMS System Design	3	0	0	3
5	18 EC 52S5	VLSI for Wireless Communication	3	0	0	3
Elective-4						
1	18 EC 52T1	Optimization Techniques and Applications in VLSI Design	3	0	0	3
2	18 EC 52O1	CMOS RF Circuit Design	3	0	0	3
3	18 EC 52T2	Advanced Digital IC Design	3	0	0	3
4	18 EC 52T3	Nano Sensors and its applications	3	0	0	3
5	18 EC 52T4	ASIC Design Flow	3	0	0	3

2018-19 (Semester I)									
S.NO	**COURSE CODE**	**COURSE NAME**	**Cos**	**COURSE OUTCOME**	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**
1	18EC5131	IC Fabrication	1	Ability to understand the Concepts of fabrication and steps following for fabrication	1				
			2	Understand different modelling technologies and materials used for fabrication		2			
			3	Ability to understand the concepts of lithography and deposition		2			
			4	Analyze the various etching technologies for preparation of ICs		2			
2	18EC5130	HDL & PLD Architectures	1	Understand the basics concepts of digital system design, their modeling techniques in Verilog HDL.			1		
			2	Design of various Combinational & Sequential Logic realizations using Verilog HDL.			2		
			3	Compare and analysis of different PLD's and CPLD's architectures.			2		
			4	Memorize and analysis of different FPGA architectures.			2		
			5	Create and Analysis of digital modules through project oriented approach					3
3	18EC5128	MOS CIRCUIT DESIGN	1	Understand basic concepts of VLSI design flow, Design styles, IC fabrication and layout design rules for CMOS circuits		1			
			2	Understand and Analyze MOS device operation, second order effects, and concepts related to scaling.		2			
			3	Analyze inverter circuits with different loads. Understand the effect of parasitic on circuit performance.		2			
			4	Understand and design Combinational and Sequential MOS logic Circuits. Analyze different Dynamic logic circuits		2			
			5	Design of Various CMOS Circuits					3
4	18EC5129	ALGORITHMS FOR VLSI DESIGN	1	Ability to understand the Concepts of design methodologies in routing and layout	2				
			2	Understand different levels of modelling of digital circuits and scheduling	2				
			3	Ability to understand the FPGA Technologies for development of physical design				2	
			4	Analyze the routing and distribution of cells in ICs				2	
5	18EC51Q4	Nano	1	Ability to understand the Concepts nano Electronics	2				

		Electronics	2	Understand different Architectures and equipment for nano electronics	2				
			3	Ability to understand the spintronics		2			
			4	Analyze the various memory devices and sensors in nano electronics		2			
6	18EC51R3	Semiconductor Device Modeling	1	Understand the basic device physics and study of MOS capacitor		2			
			2	Understand and study of MOSFET physics and characteristics.		2			
			3	Understanding the energy band diagrams of BJT and time dependent analysis.		2			
			4	Understanding the concepts of designing of emitter, base and collector and study of modern BJT.		2			
7	**18 IE 5149**	**Seminar**							
2018-19 (Semester II)									
1	18EC5232	Advanced Analog IC Design	1	Understand the operation of different current mirrors	2				
			2	Analyze the frequency response of different Amplifiers.				2	
			3	Design of two stage Op-Amp using single stage Op-Amp				2	
			4	Describe the various Feedback topologies.	2				
			5	Understand and apply the concepts of Non Linear Analog circuits.	2				
2	18EC5233	Low Power VLSI Circuits	1	Understand the physics of power dissipation including short circuit power, dynamic power and leakage power, techniques that makes a low power circuit and introduction to simulation power analysis		2			
			2	Analyse probabilistic power analysis and apply low power techniques at circuit level for CMOS circuits		2			
			3	Apply low power techniques at gate level, architecture level and system levels		2			
			4	Understand essential tasks in algorithm and architecture level low power design environments and Apply low power clock tree distribution techniques to create low power devices		2			
			5	Design of Various Low Power Circuits					2
3	18EC5234	VLSI System Design	1	Ability to understand the importance Programmable devices in VLSI			2		
			2	Understand difference between Data path sub system and array subsystem			2		
			3	Ability to understand the methodology of interconnects				2	
			4	Analyze synchronization of clock and synthesis of different disigns				2	

4	18EC5235	Testing of VLSI Circuits	1	Understanding and application user-defined primitives in Fault dominance, understanding various simulation and Gate level event-driven simulation for digital circuits.		2			
			2	Understanding, Test generation for various Combinational logic circuits and ability to design its Testable Combinational circuits.		2			
			3	Design for Testability, Generic scan based design and Classical scan based design			2		
			4	Analyze and ability to Testable various BIST– MBIST, LBIST. Fault Diagnosis of digital circuits and Diagnosis by UUT reduction.			2		
5	18EC52S3	ADVANCED VLSI DESIGN		UNDERSTAND THE CONCEPTS OF MOS CIRCUIT DESIGN	1				
				Analyze different types of buffers in mos circuits		2			
				Analyze the layouts of MOS circuits		2			
				Analyze total circuit design of MOS circuits			2		
6	18EC52T4	ASIC Design Flow		Develop Program of different logic circuits using Verilog Programming and analyze different types of Faults in logic circuits.	2				
				Analyze different types of ASIC design methodologies and Different CPLD		2			
				Analyze ASIC design flow of customized ASICs		2			
				Analyze Physical design flow of ASIC, Extraction the final circuit		2			
7	**18 IE 5250**	**Term Paper**							

Syllabus

MOS CIRCUIT DESIGN

Course Code :18 EC 5128 **L-T-P : 3-1-2**
Pre-requisite: NIL **Credits: 5**

Syllabus:

Introduction: Classification of CMOS digital circuits and Circuit design, Overview of VLSI design methodologies, VLSI design flow, Design hierarchy and concepts, VLSI design styles, Design quality, Packing technology, CAD technology, Fabrication process flow, CMOS n-well process, layout design rules. **MOS Transistor and Circuit Modeling:** MOS structure, MOS system under external bias, structure and operation of MOS transistor, MOSFET current-voltage characteristics, MOSFET scaling and small-geometry effects, MOSFET capacitances, Modeling of MOS transistor using SPICE. **MOS Inverter static characteristics and Interconnect Effects:** Introduction, Resistive-Load Inverter, Inverter with n-type MOSFET load, CMOS Inverter, Delay-Time Definitions, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters. **Combinational and Sequential MOS logic Circuits:** Introduction, MOS logic circuits with depletion nMOS loads, CMOS logic Circuits, Complex logic circuits, CMOS transmission gates (Pass gates), Behavior of bistable elements, SR latch circuit, clocked latch and flip-flop circuits, CMOS D-latch and Edge-triggered flip-flop. **Dynamic logic Circuits:** Basic principles of pass transistor circuits, voltage bootstrapping, synchronous dynamic circuit techniques, Dynamic CMOS circuit techniques, High-performance dynamic CMOS circuits.

TEXT BOOKS

1. Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits” TMH 2003
2. Neil H. E. Weste and David. Harris Ayan Banerjee,, “CMOS VLSI Design” - Pearson Education, 1999.

REFERENCES

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, “Digital Integrated Circuits” Pearson Education, 2003
2. Uyemura, “Introduction to VLSI Circuits and Systems” Wiley-India, 2006.
3. Wayne Wolf, “Modern VLSI Design ", 2nd Edition, Prentice Hall,1998.
4. Kamran Ehraghian, Dauglas A. Pucknell and Sholeh Eshraghiam, “Essentials of VLSI Circuits and Systems” – PHI, EEE, 2005 Edition.

SIMULATION BOOKS

1. Etienne Sicard, Sonia Delmas Bendhia, “Basics of CMOS Cell Design”, TMH, EEE, 2005.

ALGORITHMS FOR VLSI DESIGN AUTOMATION

Course Code :18 EC 5129 **L-T-P : 3-1-0**
Pre-requisite: NIL **Credits: 4**

Syllabus:

Introduction to Design Methodologies: Design Automation tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems
Layout: Compaction, Placement, Floor planning and Routing Problems, Concepts and Algorithms **Modeling:** Gate Level Modeling and Simulation, Switch level modeling and simulation, Basic issues and Terminology, Binary – Decision diagram, Two – Level Logic Synthesis. **Hardware Models:** Internal representation of the input algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High – level Transformations. **FPGA technologies:** Physical Design cycle for FPGA's partitioning and routing for segmented and staggered models. MCM technologies, MCM physical design cycle, Partitioning, Placement – Chip array based and full custom approaches, Routing –Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, routing and programmable MCM's.

TEXT BOOKS
1. S.H.Gerez, "Algorithms for VLSI Design Automation", John Wiley 1999.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation" 3rd edition, Springer International Edition.

REFERENCES
1. Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI" Wiley,1993
2. Wayne Wolf, "Modern VLSI Design: Systems on silicon" Pearson Education Asia, 2nd Edition.

HDL & PLD ARCHITECTURES

Course Code :18 EC 5130 **L-T-P : 3-1-2**
Pre-requisite: NIL **Credits: 5**

Syllabus:

Introduction to Verilog HDL: Basic concepts, Design modeling, Tasks and functions, Timing and delays, user-defined primitives, PLI, Simulation and Synthesis Tools.**Synthesis of Combinational & Sequential Logic:** Decoders and encoders, Multiplexers and Demultiplexers, Priority encoder, Priority decoder, Comparators, Adders, synthesis of three-state devices and bus interfaces. **,** Latches & Flip-flops, counters, registers, explicit state machines, implicit state machines. **Programmable Logic Devices:** Full Custom Design, Semicustom Design, Programmable Logic Devices, Read Only Memory (ROM), Programmable Read Only Memory (PROM), and Programmable Logic Array (PLA), and Programmable Array Logic (PAL).

Complex Programmable Logic Devices : Basic Architecture, XC9500 CPLD, GAL, Altera series – Max 5000, Max 7000 Series , ALTERA FLEX Logic – 10000 Series CPLDs. AMD's – CPLD (Mach 1 to 5).**Field Programmable Gate Arrays:** Introduction, Basic Architecture, Design flow, Xilinx XC3000 & XC4000 Architectures, Actel Architectures, ALTERA's FLEX 8000, and ALTERA's FLEX 10000 FPGAs.

TEXT BOOKS

1.Michael D.Celetti "Advanced Digital Design with the Verilog HDL" Prentice Hall.
2.S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publications.

REFERENCE BOOKS

1. Verilog Digital System Design RT Level synthesis TestBench and verification by Zainalabedin Navabi, 2008 Mc Graw Hill Publishers
2.Stephen Brown Zvonko Vranesic "Fundamentals of Digital Logic with VHDL Design" McGraw-Hill.

SIMULATION BOOKS

1. Verilog HDL A Guide To Digital Design And Synthesis, Edition: 2 by Samir Palnitkar.

IC FABRICATION TECHNOLOGY

Course Code :18 EC 5131 **L-T-P : 3-1-0**
Pre-requisite: NIL **Credits: 4**

Syllabus:

Introduction to IC Technology: Basic fabrication steps and their Importance. **Environment of IC Technology:** Concepts of Clean room and safety requirements, Concepts of Wafer cleaning processes and wet chemical etching techniques. **Impurity Incorporation:** Solid State diffusion modeling and technology; Ion Implantation modeling, technology and damage annealing, characterization of Impurity profiles **Oxidation:** Kinetics of Silicon dioxide growth both for thick, thin and ultra thin films, Oxidation technologies in VLSI and ULSI, Characterization of oxide films, High k and low k dielectrics for ULSI. **Lithography:** Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI, Mask generation. **Chemical Vapour Deposition Techniques:** CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; **Epitaxial growth of silicon:** modeling and technology. **Metal Film Deposition:** Evaporation and sputtering techniques, Failure mechanisms in metal interconnects Multi-level metallization schemes. **Plasma and Rapid Thermal Processing:** PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI.

TEXT BOOKS

1. S.M.Sze(2nd Edition)"VLSI Technology", McGraw Hill Companies Inc.

2. C.Y. Chang and S.M.Sze (Ed), **"**ULSI Technology**"**, McGraw Hill Companies Inc.

REFERENCES TEXT BOOKS

1.Stephena, Campbell, **"**The Science and Engineering of Microelectronic Fabrication**"**, Second Edition, Oxford University Press.

2.James D.Plummer, Michael D.Deal, "Silicon VLSI Technology" Pearson Education

EMBEDDED SYSTEM DESIGN

Course Code :18 EC 51Q1 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Introduction to Embedded systems: Embedded systems, processor embedded into a system, embedded hardware units and devices in a system, embedded software in a system, examples of embedded systems, embedded SOC and use of VLSI circuit design technology, Complex systems design and processors, Design process in embedded system, formalization of system design, design process and design examples, classification of embedded systems, skills required for an embedded system designer. **PIC Microcontrollers**: PIC 16 Series family overview, An architecture overview of the 16F84A, Status register, 16F84A memory, Some issues of timing, Power-up and Reset, PIC 16F84A parallel ports, 16F84A clock oscillator, 16F84A operating conditions, 16F84A interrupt structure. **Larger systems and the PIC 16F873A:** The main idea – the PIC 16F87XA, The 16F873A block diagram and CPU, 16F873A memory and memory maps, 16F873A interrupts, 16F873A oscillator, reset and power supply, 16F873A parallel ports. **RTOS:** Basic design using RTOS, Micro/OS-II and V_x works, windows CE, OSEK, real-time Linux functions, **case study:** digital camera hardware and software architecture, embedded systems in automobile, embedded system for a smart card, mobile phone software for key inputs.

TEXTBOOKS

1. Embedded Systems Architecture Programming and Design by Raj Kamal, II edition, Tata MC Graw-Hill.
2. Designing Embedded Systems with PIC Microcontrollers: principles and applications by Tim Wilmshurst, Elsevier.

REFERENCES

1. Embedded Systems Design by Steve Heath, II edition, Newnes publications
2. Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers by Tammy Noergaard, Elsevier.

SIMULATION BOOKS

1. An embedded software primer by David E. Simon, Pearson Education, 1995.

VLSI SIGNAL PROCESSING

Course Code :18 EC 51Q2 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Introduction To DSP Systems: Introduction; representation of DSP algorithms: Block Diagram, signal flow graph, data flow graph, dependence graph. **Iteration Bound**: Data flow graph representations, loop bound and iteration bound, longest path matrix algorithm, iteration bound of Multirate data flow graphs. **Pipelining and Parallel Processing:** Pipelining and parallel processing of FIR digital filters, pipeline interleaving in digital filters: signal and multichannel interleaving. **Retiming, Unfolding and Folding**: retiming techniques; algorithm for unfolding, Folding transformation, systolic architecture design, systolic array design methodogy. **Fast Convolution, Filters and Transforms**: Cook-toom algorithm, modified cook-toom algorithm, winogard algorithm, iterated convolution Algorithm strength reduction in filters and transforms.

TEXT BOOK
1.Keshab k. Parhi," VLSI Digital Signal Processing Systems: Design and Implementation", Wiley, inter science.

REFERENCE BOOKS
1.S.Y.kung, H.J.White house, T. Kailath," VLSI and Modern Signal Processing", Prentice hall,

CMOS MIXED SIGNAL CIRCUITS
Course Code :18 EC 51Q3 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Data Converter Modeling and SNR: Sampling and Aliasing: A modeling Approach, SPICE models for DACs and ADCs, Quantization noise, Viewing the quantization noise spectrum using simulations, quantization noise voltage spectral density, Data converter SNR: an overview, Improving SNR using averaging, Decimating filters for ADC, Interpolating filters for DACs, Using feedback to improve SNR. **Submicron CMOS Circuit Design:** Submicron CMOS overview and models, Digital circuit design, Analog circuit design. **Implementing Data Converters:** R-2R topologies for DACs, Op-Amps in data converters, Implementing ADCs. **Noise-Shaping Data Converters:** Noise-shaping fundamentals, Second-order noise-shaping, noise-shaping topologies. **Integrator-Based CMOS Filters:** Integrator building blocks, filtering topologies, Filters using Noise-shaping.

TEXT BOOKS
1 R. Jacob Baker, "CMOS: Mixed-Signal Circuit Design", Wiley-Student Edition, IEEE Press,

REFERENCE BOOKS

1. Behzad Razavi, "Principles of Data Conversion System Design, "John Wiley & Sons.
2.P. Allen and D. Holberg, "CMOS Analog Circuit design," Oxford Press.
3. E. Bogatin, "Signal and Power –Simplified," 2nd edition, Prentice Hall.

NANO ELECTRONICS

Course Code :18 EC 51Q4 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Introduction: Recent past, the present and its challenges, Future, Overview of basic Nano electronics. **Nano electronics & Nanocomputer architectures:** Introduction to Nanocomputers, Nanocomputer Architecture, Quantum DOT cellular Automata (QCA), QCA circuits, Single electron circuits, molecular circuits, Logic switches – Interface engineering – Properties (Self-organization, Size-dependent) – Limitations. **Nanoelectronic Architectures:** Nanofabrication – Nanopatterning of Metallic/Semiconducting nanostructures (e-beam/X-ray, Optical lithography, STM/AFM- SEM & Soft-lithography) – Nano phase materials – Self-assembled Inorganic/Organic layers. **Spintronics:** Introduction, Overview, History & Background, Generation of Spin Polarization Theories of spin Injection, spin relaxation and spin dephasing, Spintronic devices and applications, spin filters, spin diodes, spin transistors. **Memory Devices And Sensors:** Memory devices and sensors – Nano ferroelectrics – Ferroelectric random access memory –Fe-RAM circuit design –ferroelectric thin film properties and integration – calorimetric -sensors – electrochemical cells – surface and bulk acoustic devices – gas sensitive FETs – resistive semiconductor gas sensors –electronic noses – identification of hazardous solvents and gases – semiconductor sensor array

TEXT BOOKS

1.Nanoelectronics & Nanosystems: From Transistor to Molecular & Quantum Devices: Karl Goser,
JanDienstuhl and others.
2. Nano Electronics and Information Technology: Rainer Waser

REFERENCES

1. Concepts in Spintronics – Sadamichi Maekawa
2. Spin Electronics – David Awschalom

CAD TOOLS FOR VLSI

Course Code :18 EC 51Q5 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Introduction to VLSI design methodologies and supporting CAD environment. **Schematic editors:** Parsing: Reading files, describing data formats, Graphics & Plotting Layout. Layout Editor: Turning plotter into an editor. Layout language: Parameterized cells, PLA generators, Introduction to Silicon compiler, Data path. Compiler, Placement & routing, Floor planning. Layout Analysis: Design rules, Object based DRC, Edge based layout operations. Module generators. **Simulation:** Types of simulation, Behavioral simulator, logic simulator, functional simulator & Circuit simulator. Simulation Algorithms: Compiled code and Event-driven. **Optimization Algorithms:** Greedy methods, simulated annealing, genetic algorithm and neural models. **Testing ICs:** Fault simulation, Aids for test generation and testing. Computational complexity issues: Big Oh and big omega terms. **Recent topics in CAD-VLSI:** Array compilers, hardware software co-design, high-level synthesis tools and VHDL modeling.

TEXT BOOKS

1. Stephen Trimberger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002
2. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher,
Second edition.

REFERENCE BOOKS

1.Gaynor E. Taylor, G. Russell, "Algorithmic and Knowledge Based CAD for VLSI", Peter peregrinus ltd.
London.
2. Gerez, "Algorithms VLSI Design Automation", John Wiley & Sons.

IMAGE AND VIDEO PROCESSING

Course Code :18 EC 51R1 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Fundamentals of Image processing and Image Transforms: Basic steps of Image processing system sampling and quantization of an Image – Basic relationship between pixels Image Transforms: 2 – D Discrete Fourier Transform, Discrete Cosine Transform (DCT), Discrete Wavelet transforms **Image Processing Techniques:** Image Enhancement: Spatial Domain methods: Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial filters, Sharpening Spatial filters Frequency Domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, selective filtering Image Segmentation: Segmentation concepts, point, line and Edge detection, Thresholding, region based segmentation **Image Compression** Image compression fundamentals – coding Redundancy, spatial and temporal

redundancy. Compression models : Lossy and Lossless, Huffmann coding, Arithmetic coding, LZW coding, run length coding, Bit Plane coding, transform coding, predictive coding , wavelet coding, JPEG standards **Basic Steps of Video Processing:** Analog video, Digital Video, Time varying Image Formation models : 3D motion models, Geometric Image formation , Photometric Image formation, sampling of video signals, filtering operations **2-D Motion Estimation:** Optical flow, general methodologies, pixel based motion estimation, Block matching algorithm, Mesh based motion Estimation, global Motion Estimation, Region based motion estimation, multi resolution motion estimation. Waveform based coding, Block based transform coding, predictive coding, Application of motion estimation in video coding.

TEXT BOOKS

1. Gonzaleze and Woods ,"Digital Image Processing ", 3rd edition , Pearson
2. Yao wang, Joem Ostarmann and Ya – quin Zhang, "Video processing and communication ",1st edition ,
   PHI

REFERENCE TEXT BOOK

1. M. Tekalp ,"Digital video Processing", Prentice Hall International

SIMULATION TEXT BOOKS

1. Relf, Christopher G.,"Image acquisition and processing with LabVIEW", CRC press
2. Aner ozdemi R, "Inverse Synthetic Aperture Radar Imaging with MATLAB Algorithms", John Wiley &
   Sons
3. Chris Solomon, Toby Breckon ,"Fundamentals of Digital Image Processing A Practical Approach with Examples in Matlab", John Wiley & Sons,

BiCMOS TECHNOLOGY & APPLICATIONS

Course Code :18 EC 51R2 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Device Modeling: Modeling of the MOS Transistor, Modeling of the Bipolar Transistor. **Device Design Considerations:** Design Considerations for MOSFET's, Design Considerations for Bipolar Transistors, BiCMOS Device Synthesis. **BiCMOS Device Scaling:** MOS Device Scaling, Bipolar Device Scaling. **BiCMOS Process Technology:** BiCMOS Isolation Consideration, CMOS Well & Bipolar Collector tradeoffs, CMOS & BiCMOS Processes considerations, Interconnect Processes for submicron BiCMOS, Submicrometer BiCMOS Process for 5V Digital Applications, Analog BiCMOS Process Technology, Process Reliability. **Digital Design:** Delay Analysis, Gate Design, Performance Comparisons. **Analog Design:** BiCMOS Operational Amplifiers, BiCMOS Analog Subsystems**. BiCMOS Digital Circuit Applications**: Adders, Multiplier, Random Access Memory, Programmable Logic Arrays, BiCMOS Logic Cells, BiCMOS Gate Arrays.

TEXT BOOKS:

1. A L ALVAREZ, BICMOS Technology & Applications, Kluwer Academic Publishers.
2. Sherif H.K. Embabi, Abdellatif Bellaouar & Mohamed 1. Elmasry "Digital BiCMOS Integrated Circuit Design" Springer Science+ BusÎness Media, LLC.

REFERENCE

1. Kiat-Seng yeo, Samir S. Rofail, Wang-Ling Goh, CMOS/BiCMOS ULSI, Pearson Education.
2. James C. Daly, Denis P. Galipeau, Analog BiCMOS Design: Practices & Pitfalls, CRC Press
3. Klaas-Jan de Langen, Johan Huijsing, Compact Low-Voltage and High-Speed CMOS, BiCMOS and Bipolar Operational Amplifiers, Springer Science

SEMICONDUCTOR DEVICE MODELING

Course Code :18 EC 51R3 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Basic Device Physics : Electrons and holes in silicon, p-n junction, MOS capacitor, Highfield effects. **MOSFET Devices** : Long-channel MOSFETs, Short-channel MOSFETs. CMOS Device Design : MOSFET Scaling, Threshold voltage, MOSFET channel length. **CMOS Performance Factors** : Basic CMOS circuit elements, Parasitic elements, Sensitivity of CMOS delay to device parameters, Performance factors of advanced CMOS devices. **Bipolar Devices** : n-p-n Transistors, Ideal current-voltage characteristics, Characteristics of a typical n-p-n transistor, Bipolar device models for circuit and time-dependent analyses, Breakdown voltages. **Bipolar Device Design** : Design of the emitter design, Design of the base region, Design of the collector design, Modern bipolar transistor structures.

TEXT BOOKS

1. Yuan Taur, Tak.H.Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press,

REFERENCE BOOKS

1. Donald Neamen, Semiconductors Physics and Devices, Tata Mc Graw Hill, 2003
2. Tyagi, Introduction to Semiconductor Materials and Devices, Wiley Publications, 2002.
3. Semiconductor Devices, Basic Principles Jasprit Singh, Wiley Publications, 2001
4. S.M. Sze (Ed), Physics of Semiconductor Devices, 2nd Edition, Wiley Publications, 1998
5. Analysis and Design of Analog Integrated Circuits 4/e, Paul R. Gray, Paul J. Hurst, Robert G Meyer, 2001, Wiley Publications
6. Physics of Semiconductor Devices 3/e S. M. Sze, Wiley Publications, 2007.

MEMORY DESIGN AND TESTING

Course Code :18 EC 51R4 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Random Access Memory Technologies-Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar, SRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies- Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures- BiCMOS DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs. **Non-Volatile Memories-**Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)- Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating- Gate EPROM Cell-One-Time Programmable (OTP) Eproms-Electrically Erasable PROMs (EEPROMs)- EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture. **Memory Fault Modeling, Testing, And Memory Design For Testability And Fault Tolerance-**RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing. **Semiconductor Memory Reliability And Radiation Effects-**General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimeter-Water Level Radiation Testing and Test Structures. **Advanced Memory Technologies And High-Density Memory Packaging Technologies-**Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magneto resistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

TEXT BOOKS

1.Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ", Prentice-Hall of India Private Limited, New Delhi, 1997.

REFERENCE BOOKS

1. Luecke Mize Care, “Semiconductor Memory design & application”, Mc-Graw Hill.
2.Belty Prince, “ Semiconductor Memory Design Handbook”.
3.Memory Technology design and testing 1999 IEEE International Workshop on: IEEE Computer Society Sponsor (S).

RECONFIGURABLE COMPUTING

Course Code :18 EC 51R5 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Introduction Goals and motivations - History, state of the art, future trends - Basic concepts and related fields of study - Performance, power, and other metrics - Algorithm analysis and speedup projections - RC Architectures - Device characteristics - Fine-grained architectures - Coarse-grained architectures . **Fpga Design** FPGA Physical Design Tools -Technology mapping - Placement & routing - Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization .**Parallel Processing** RC Application Design - Parallelism - Systolic arrays - Pipelining - Optimizations - Bottlenecks - High-level Design - High-level synthesis - High-level languages - Design tools. **Architectures** Hybrid architectures- Communication - HW/SW partitioning - Soft-core microprocessors- System architectures -System design strategies - System services - Small-scale architectures - HPC architectures - HPEC architectures - System synthesis - Architectural design space explorations. **Case Study** Case Studies- Signal and image processing - Bioinformatics - Security - Special Topics - Partial Reconfiguration - Numerical Analysis -Performance Analysis/Prediction - Fault Tolerance

TEXT BOOK

1. Paul S. Graham and Maya Gokhale "Reconfigurable Computing Accelerating Computation with Field-Programmable Gate Arrays" springer .

ADVANCED ANALOG IC DESIGN

Course Code :18 EC 5232 **L-T-P : 3-1-2**
Pre-requisite: NIL **Credits: 5**

Syllabus:

Small Signal & large signal Models of MOS & BJT transistor. Analog MOS Process **Passive & Active Current Mirrors:** Basic current mirrors, Cascode current mirror, Active loads, voltage and current references; **Frequency response of integrated circuits:** Single Stage (CS,CG,CD) amplifiers, Cascade Stage; frequency response(miller effect) of CG, CS, CD, Operation of Basic Differential Pair, differential pair with MOS loads, Frequency response of Cascade & Differential Pair; **Operational Amplifiers with single ended outputs:** Applications of operational amplifiers, basic two stage MOS operational amplifiers, Deviations from ideality in real operational amplifiers, Basic two-stage MOS operational amplifier, MOS Folded – cascode operational amplifiers, **Feedback**: Ideal feedback equation, gain sensitivity, feedback configurations, practical configuration and effect of loading **Nonlinear Analog circuits & other applications:** Precision rectification ,phased locked loops, Sampling Switches, switched capacitor integrator, oscillators, ADC, DAC.

TEXT BOOKS

1. Gray & Meyer, Analysis & Design of Analog Integrated Circuits, 4th edition, Wiley, 2001.
2. Behzad Razavi, "Design Of Analog CMOS Integrated Circuits", Tata Mcgraw Hill,2005.

REFERENCE

1. Jacob Baker,"CMOS Mixed Signal Circuit Design", John Wiley.
2. Gray, Wooley, Brodersen, " Analog MOS Integrated Circuits ", IEEE Press, 1989.
3. Kenneth R. Laker, Willy M.C. Sansen, William M.C.Sansen, "Design of Analog Integrated Circuits and
Systems ", McGraw Hill.

LOW POWER VLSI CIRCUITS

Course Code :18 EC 5233 **L-T-P : 3-0-2**

Pre-requisite: NIL **Credits: 4**

Syllabus:

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. **Device & Technology Impact on Low Power:** Dynamic dissipation in CMOS, Transistor sizing& gate oxide thickness, Impact of technology Scaling, Technology & Device innovation. **Simulation Power analysis**: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation. **Probabilistic power analysis**: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. **Low Power Circuit's**: Transistor and gate sizing, network restructuring and Reorganization. Special Flip Flops & Latches design, high capacitance nodes, low power digital cells library. **Logic level:** Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. **Low power Architecture & Systems:** Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components. **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network. **Special Techniques**: Power Reduction in Clock networks, CMOS Floating Node, Low Power Bus Delay balancing, and Low Power Techniques for SRAM.

TEXT BOOKS

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002
2. Rabaey, Pedram, "Low Power Design Methodologies" Kluwer Academic

REFERENCES

1. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000
2. Yeo, "CMOS/BiCMOS ULSI Low Voltage Low Power" Pearson Education

VLSI SYSTEM DESIGN

Course Code :18 EC 5234 **L-T-P : 3-1-0**

Pre-requisite: NIL **Credits: 4**

Syllabus:

Design Methodology: Structured design techniques; Programmable logic; Gate array and sea of gates design; cell based design; full custom design; Design flow; Design Economics. **Data path**

Subsystems: Adders; One/zero Detectors; Comparators; Counters; Shifters; Multipliers; Power and Speed Trade-off. **Memory and Array Subsystems:** SRAM, DRAM, ROM, Serial access memories; CAM, PLAs; Array yield, reliability; Power dissipation in Memories. **Special-purpose Subsystems:** Packaging; power distribution; I/O pads; **Interconnect:** Interconnect parameters; Electrical wire models, capacitive parasitics; Resistive parasitics; Inductive parasitic; Crosstalk; Advanced Interconnect Techniques. **Timing Issues:** Timing classification; Synchronous design; Self-timed circuit design; **Clock Synthesis and Synchronization:** Synchronizers; Arbiters; Clock Synthesis; PLLs; Clock generation; Clock distribution; Synchronous Vs Asynchronous Design.

TEXT BOOKS

1. Neil H. E. Weste, David. Harris and Ayan Banerjee,, "CMOS VLSI Design" - Pearson Education, Third Edition, 2004.
2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits" Pearson Education, Second Edition.

REFERENCES:

1. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits" TMH, Third Edition, 2003
2 Wayne Wolf, "Modern VLSI Design ", 2nd Edition, Prentice Hall,1998.

SIMULATION BOOKS

1. Etienne Sicard, Sonia Delmas Bendhia, "Basics of CMOS Cell Design", TMH, EEE, 2005.

TESTING OF VLSI CIRCUITS

Course Code :18 EC 5235 **L-T-P : 3-1-0**
Pre-requisite: NIL **Credits: 4**

Syllabus:

Basics of Testing And Fault Modeling Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation. **Test Generation For Combinational and Sequential Circuits** Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits. **Design For Testability** Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design – System level DFT approaches. **Self Test and Test Algorithms** Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs. **Fault Diagnosis Logic** Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

TEXT BOOKS

1.M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico
Publishing House.
2.M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal
VLSI Circuits", Kluwer Academic Publishers.

REFERENCE BOOKS

1.P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
2.A.L. Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International.

SYSTEM ON CHIP DESIGN

Course Code :18 EC 52S1 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

System Level Design: System level design-Tools & methodologies for system level design, System level space & modeling languages, SOC block based design & IP assembly, Performance evaluation methods for multiprocessor SOC design, **Power Management And Synthesizing** System level power management, Processor modeling & design tools, Embedded software modeling & design Using performance metrics to select microprocessor for IC design, Parallelizing High-Level Synthesize ,A code transformational approach to High Level Synthesize.
Micro-Architecture Design And Power Optimization Micro-architecture design, Cycle accurate system – level modeling, Performance evaluation, Micro architectural power estimation optimization, Design planning. **Software Design Verification** logical verification, Design & Verification languages, Digital simulation, using transactional, level models in an SOC design, Assertion based verification. **Hardware Design Verification** Hardware acceleration & emulation, Formal property verification, TEST, DFT, ATPG,Analog
& mixed signal test

TEXT BOOK
1. Louis Scheffer Luciano Lavagno and Grant Martin, "EDA for IC System verification and Testing", CRC,
2006.

REFERENCES
1.Wayone Wolf," Modern VLSI Design: SOC Design"
2.Prakash Rashnikar, Peter Paterson, Lenna Singh" System-On-A-Chip Verification methodlogy &
Techniques", Kluwer Academic Publishers.
3.Alberto Sangiovanni Vincentelli," Surviving the SOC Revolution: A Guide to Platformbased Design",
Kluwer Academic Publishers

PROCESS AND DEVICE CHARACTERIZATION & MEASUREMENTS

Course Code :18 EC 52S2 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Introduction And Preliminary Concepts: Macro-Meso, Micro and Nanostructure of Materials, Fundamentals of crystallography and Crystal structures Optical Microscopy: Geometry of Optics, Resolution, and Construction of a Microscope, Image Contrast, and Phase Contrast. **Electron Microscopy**: SEM: Electron Optics - Interaction of Electrons and Matter - Elastic and Inelastic Scattering, Backscattered Electrons, Secondary Electrons, Scanning Electron Microscopy – Image Formation, EPMA, Magnification, and Depth of Field, Distortion, Detectors, Contrast, and Resolution. TEM: Electron diffraction, different electron Diffraction techniques. **Semiconductor Material Impurity Characterization**: Spectroscopic Ellipsometry (SE), X-ray Reflectivity (XRR), X-ray Fluorescence (XRF), X-ray Diffraction (XRD), Secondary Ion Mass Spectrometry (SIMS), Auger Electron Spectrometry (AES), Rutherford Backscattering Spectrometry (RBS), EDAX, FTIR. **Electrical Characterization**: Four-probe technique, Hall Effect, sheet resistance C-V measurements, DLTS, Carrier lifetime, impurity profiling, I-V measurements . **Process And Spice Model Parameter Extraction**

TEXT /REFERENCES

1) W.R. Reunyan, "Semiconductor Measurements and Instrumentation", Mc-Graw Hill
2) Micro structural Characterization of Materials - David Brandon and Wayne Kaplan, John Wiley and
Sons, New York, NY.
3) Schroder, "Semiconductor Material and Device Characterization"
4) Philips F. Kare and Greydon B. Lauabee, "Characterization of semiconductor Materials", Mc-Graw Hill.
5) K.V. Ravi, "Imperfections and Impurities in Semiconductor Silicon", John Wiley and Sons.

ADVANCED VLSI DESIGN

Course Code :18 EC 52S3 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Review of MOS Circuits: MOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS. **MESFETS**: MESFET and MODFET operations, quantitative description of MESFETS. **MIS Structures and MOSFETS**: MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS. **Short Channel Effects and Challenges to CMOS**: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization **Beyond CMOS**: Evolutionary advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic ,Defect tolerant computing. **Super Buffers, Bi-CMOS and Steering Logic**: Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks - NMOS and CMOS functional blocks. **Special Circuit Layouts and Technology Mapping**: Introduction, Talley circuits, NAND-NAND, NORNOR, and AOI Logic, NMOS, CMOS

Multiplexers, Barrel shifter, Wire routing and module lay out. **System Design**: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom Design.

TEXT BOOKS

1. Kevin F Brennan **"**Introduction to Semi Conductor Device**"**, Cambridge publications
2. Eugene D Fabricius **"**Introduction to VLSI Design**"**, McGraw-Hill publications

REFERENCE BOOKS

1. D.A Pucknell **"**Basic VLSI Design**"**, PHI Publication
2. Wayne Wolf, **"**Modern VLSI Design**"** Pearson Education, Second Edition

MEMS SYSTEM DESIGN

Course Code :18 EC 52S4 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

MEMS and Microsystems, Microsystems and microelectronics, Microsystems and miniaturization, Working principle of micro system - Micro sensors, Micro actuators, MEMS with Micro actuators. **Materials For MEMS** - Substrate and wafer, silicon as a substrate material, silicon compound, silicon Piezo-resistors, Gallium Arsenide, quartz, Piezoelectric crystals, polymers and packaging Materials. **Fabrication Process** - Photolithography, Ion implantation, Oxidation, Chemical vapor deposition (CVD), Physical vapor deposition, Deposition by Epitaxy, Etching. **Manufacturing Process** - Bulk Micromachining, Surface Micromachining, LIGA Process. Micro system Design - Design consideration, process design, Mechanical design, Mechanical design using MEMS. **Mechanical packaging of Microsystems**, Microsystems packaging, interfacing in Microsystems packaging, packaging technology, selection of packaging materials, signal mapping and transduction. **Case study on strain sensors**, Temperature sensors, Pressure sensors, Humidity sensors, Accelerometers, Gyroscopes , RF MEMS Switch, phase shifter, and smart sensors. Case study of MEMS pressure sensor Packaging.

TEXTBOOKS

1.Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.
2.Julian W Gardner, "Microsensors MEMS and smart devices", John Wiley and sons Ltd,2001.
3.Chang Liu, "Foundation of MEMS", Pearson International Edition,2006.

REFERENCES

1.Stephen Santuria," Microsystems Design", Kluwer publishers, 2000.
2.Nadim Maluf," An introduction to Micro electro mechanical system design", Artech House,
3.Mohamed Gad-el-Hak, editor," The MEMS Handbook", CRC press Baco Raton,2000.
4.Gabriel M Rebeiz, "RF MEMS - Theory Design and Technology", John Wiley and Sons, 2003.

VLSI FOR WIRELESS COMMUNICATION

Course Code :18 EC 52S5 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Communication Concepts: Wireless Channel Description, Path Loss, Multipath Fading, Channel Model and Envelope Fading, Frequency Selective and Fast Fading **Receiver Architectures**: Receiver Front End:, Filter Design, Rest of Receiver Front End, Derivation of NF, IIP3 of Receiver Front End, **Low Noise Amplifier**: Wideband LNA Design, Narrow Band LNA:, Impedance Matching, Core Amplifier **Active Mixer**: Balancing, Qualitative Description of the Gilbert Mixer, Distortion, Low Frequency Case: Analysis of Gilbert Mixer, Distortion, High-Frequency Case, Noise **Passive Mixer**: Switching Mixer, Distortion in Unbalanced Switching Mixer, Conversion Gain in Unbalanced Switching Mixer, Noise in Unbalanced Switching Mixer, practical Unbalanced Switching Mixer, Sampling Mixer, Conversion Gain in Single-Ended Sampling Mixer **Analog-to-Digital Converters**: Demodulators, A/D converters Used in a Receiver, Low-Pass Sigma-Delta Modulators, Implementation of Low-Pass Sigma-Delta Modulators, Bandpass Sigma-Delta Modulators, Implementation of Bandpass Sigma-Delta Modulators

TEXT BOOK
1. Bosco Leung, "VLSI for Wireless Communication, Second Edition, Springer

REFERENCES
1. Emad N Farag, M.I Elmasry, “Mixed Signal VLSI Wireless Design Circuits and Systems”, KluwerPublication.
2. David Tsee, Pramod Viswanath,” Fundamentals of Wireless Communication”, Cambridge Univ Press.

OPTIMIZATION TECHNIQUES AND APPLICATIONS IN VLSI DESIGN

Course Code :18 EC 52T1 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Statistical Modeling: Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgroms model, principal component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models Statistical Performance, Power And Yield Analysis Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation Convex Optimization Convex sets,

convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Max-monomial fitting, Polynomial fitting. Genetic Algorithm Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation-Partitioning algorithm Taxonomy-Multiday Partitioning Hybrid genetic-encoding-local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm. Ga Routing Procedures And Power Estimation Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures. Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding-fitness function-GA vs Conventional algorithm.

REFERENCES

1.Ashish Srivastava, Dennis Sylvester, David Blaauw "Statistical Analysis and Optimization for VLSI:Timing and Power" , Springer, 2005.
2.Pinaki Mazumder, E.Mrudnick, "Genetic Algorithm for VLSI Design,Layout and test Automation",
Prentice Hall,1998.
3.Stephen Boyd, Lieven Vandenberghe "Convex Optimization", Cambridge University Press,

CMOS RF CIRCUIT DESIGN

Course Code :18 EC 52O1 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Introduction to RF Design and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Inter symbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion **RF Modulation:** Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures, Direct conversion and two-step transmitters **RF Testing:** RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers. **BJT and MOSFET behavior at RF Frequencies:** BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation **RF Circuits Design:** Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers-working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Design issues in integrated RF filters.

TEXT BOOKS

1. B. Razavi, "RF Microelectronics" PHI 1998
2. R. Jacob Baker, H.W. Li, D.E. Boyce "CMOS Circuit Design, layout and Simulation", PHI

REFERENCE BOOKS

1. Thomas H. Lee "Design of CMOS RF Integrated Circuits" Cambridge University press 1998.
2. Y.P. Tsividis, "Mixed Analog and Digital Devices and Technology", TMH 1996

ADVANCED DIGITAL IC DESIGN

Course Code :18 EC 52T2 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Implementation Strategies for Digital ICs: Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Prewired Arrays, Perspective—The Implementation Platform of the Future. **Coping with Interconnect:** Introduction, Capacitive Parasitics, Capacitance and Reliability—Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability—Ohmic Voltage Drop, Electromigration, Resistance and Performance—RC Delay. **Timing Issues in Digital Circuits:** Introduction, Timing Classification of Digital Systems,Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Synchronizers and Arbiters, Synchronizers— Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL. **Designing Arithmetic Building Blocks: I**ntroduction, The Adder, The Binary Adder: Definitions, The Full Datapaths in Digital Processor Architectures, Adder: Circuit Design Considerations, The Binary Adder: Logic Design Considerations, The Multiplier, The Multiplier: Definitions, Partial- Product Generation, Partial Product Accumulation, Final Addition, Multiplier Summary, The Shifter, Barrel Shifter, Logarithmic Shifter. **Designing Memory and Array Structures:** Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories, Nonvolatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers, Voltage References, Drivers/Buffers, Timing and Control.

TEXTBOOKS

1. Kamran Ehraghian, Dauglas A. Pucknell and Sholeh Eshraghiam, "Essentials of VLSI Circuits and Systems" – PHI, EEE, 2005 Edition.
2. Neil H. E. Weste and David. Harris Ayan Banerjee,, "CMOS VLSI Design" - Pearson Education.

REFERENCES

1. Sung-Mo Kang, Yusuf Leblebici,"CMOS Digital Integrated Circuits" TMH 2003
2. Jan M. Rabaey, "Digital Integrated Circuits" Pearson Education, 2003
3. Wayne Wolf, "Modern VLSI Design ", 2nd Edition, Prentice Hall,1998.

SIMULATION BOOKS

1. Etienne Sicard, Sonia Delmas Bendhia, "Basics of CMOS Cell Design", TMH, EEE, 2005.

NANO SENSORS AND ITS APPLICATIONS

Course Code :18 EC 52T3 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Sensor Characteristics And Physical Effects: Active and Passive sensors – Static characteristic - Accuracy, offset and linearity – Dynamic characteristics - First and second order sensors – Physical effects involved in signal transduction- Photoelectric effect – Photo dielectric effect – Photoluminescence effect – Electroluminescence effect – Hal effect – Thermoelectric effect – Peizoresistive effect – Piezoelectric effect – Pyroelectric effect –Magneto-mechanical effect (magnetostriction) – Magneto resistive effect. **Nano Based Inorganic Sensors:** Density of states (DOS) – DOS of 3D, 2D, 1D and 0D materials – one dimensional gas sensors:- gas sensing with nanostructured thin films – absorption on surfaces – metal oxide modifications by additives – surface modifications – nano optical sensors – nano mechanical sensors – plasmon resonance sensors with nano particles – AMR, Giant and colossal magneto resistors – magnetic tunneling junctions. **Organic / Biosensors:** Structure of Protein – role of protein in nanotechnology – using protein in nanodevices – antibodies in sensing – antibody in nano particle conjugates – enzymes in sensing – enzyme nanoparticle hybrid sensors – Motor proteins in sensing – transmembrane sensors – Nanosensors based on Nucleotides and DNA – Structure of DNA – DNA decoders and microarrays – DNA protein conjugate based sensors – Bioelectronic sensors – DNA sequencing with nanopores – sensors based on molecules with dendritic architectures – biomagnetic sensors. **Nano Sensors:**Temperature Sensors, Smoke Sensors, Sensors for aerospace and defense: Accelerometer, Pressure Sensor, Night Vision System, Nano tweezers, nano-cutting tools, Integration of sensor with actuators and electronic circuitry Biosensors. **Applications:** Cantilever array sensors - Cantilever sensors for diagnosis of diabetes mellitus - Cantilever sensors for cancer diagnosis - Nanotube based sensors - Nanotube based sensors for DNA detection - Nanotube based sensors for capnography - Nanowire based sensors - Nanowire based electrical detection of single viruses - Nanowire based electrical detection of biomolecules. **Detectors and Applications:** Bio receptors –Bio detectors - Nano array based detector - Nano Particle based detector - Ultra-sensitive detection of pathogenic biomarkers - Ultra-sensitive detection of single bacteria.

REFERENCES:

1. Kourosh Kalantar – Zadeh, Benjamin Fry, "Nanotechnology- Enabled Sensors", Springer,
2. H.Rosemary Taylor, "Data acquisition for sensor systems", Chapman & Hall, 1997.

3. Jerome Schultz, Milan Mrksich, Sangeeta N. Bhatia, David J. Brady, Antonio J. Ricco, David
4 R. Walt, Charles L. Wilkins, "Biosensing: International Research and Development", Springer,
5. Ramon Pallas-Areny, John G. Webster, "Sensors and signal conditioning" John Wiley & Sons, 2001.
6. Vijay.K.Varadan, Linfeng Chen, Sivathanupillai, "Nanotechnology Engineering in Nano and Biomedicine", John Wiley & Sons, 2010.

ASIC DESIGN FLOW

Course Code :18 EC 52T4 **L-T-P : 3-0-0**
Pre-requisite: NIL **Credits: 3**

Syllabus:

Types of ASICs – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers. **ASIC Library design**: Transistors as resistors – parasitic capacitance – logical effort programmable ASIC design software: Design system – logic synthesis – half gate ASIC. **Low level design entry:** Schematic entry – low level design languages – PLA tools – EDIF – An overview of VHDL and verilog. Logic synthesis in verilog and & VHDL simulation. **CMOS System case studies: Dynamic warp processor:** Introduction, the problem, the algorithm, a functional overview, detailed functional specification, structural floor plan, physical design, fabrication. **pixels-planes graphic engine:** introduction, raster scan graphic fundamental, pixels-planes system overview, chip electrical design, chip organization and layout, clock distribution. **Hierarchical layout and design of single chip 32 bit CPU:** Introduction ,design methodology, technology updatability and layout verification. **Floor planning & placement:** Floor Planning Goals and Objectives**,** Measurement of Delay in floor planning, Floor planning tools ,I/O and Power planning, Clock planning ,Placement Algorithms**. Routing**: Global routing, Detailed routing ,Special routing.

TEXT BOOKS

1. Application specific Integrated Circuits", J.S. Smith, Addison Wesley.
2. Principles of CMOS VLSI Design : A System Perspective, N. Westle & K. Eshraghian ,Addison – Wesley Pub.Co.1985.

REFERENCES

1. Basic VLSI Design :Systems and Circuits, Douglas A. Pucknell & Kamran Eshraghian, Prentice Hall of India Private Ltd. , New Delhi , 1989.
2. Introduction to VLSI System,C. Mead & L. Canway, Addison Wesley Pub
3. Introduction to NMOS & VLSI System Design, A. Mukharjee, Prentice Hall,
4. The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985.
5. Digital Integrated Circuits: A Design Perspective, Jan A. Rabey, Prentice Hall of India Pvt Ltd