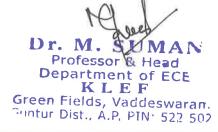
## Koneru Lakshmaiah Education Foundation (Category -1, Deemed to be University estd. u/s. 3 of the UGC Act, 1956)

Accredited by NAAC as 'A++' ◆Approved by AICTE ◆ ISO 21001:2018 Certified Campus: Green Fields, Vaddeswaram - 522 302, Guntur District, Andhra Pradesh, INDIA. Phone No. +91 8645 - 350 200; www.klef.ac.in; www.klef.edu.in; www.kluniversity.in Admin Off: 29-36-38, Museum Road, Governorpet, Vijayawada - 520 002, Ph: +91 - 866 - 3500122, 2576129

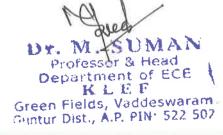
## Department of Electronics and Communication Engineering

Program: M. Tech - VLSI Academic Year 2023-2024

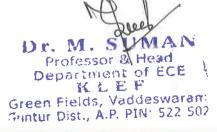
<b>Course Code</b>	Course Name	CO NO	CO Description
23VL5001	Transformation Techniques, Random Variables & Stochastic Processes	1	Apply Mathematical models of random phenomena and solve probabilistic problems.
		2	Analyze different types of random variables and compute statistical parameters of the random variables.
		3	Apply random processes in the time domain and model time-varying linear systems.
		4	Analyze random processes in frequency domains and model spectral characteristics of LTI systems.
23VL5101	MoS Circuit Design	1	Apply basic concepts of VLSI design flow, Design styles,IC fabrication ,layout design rules for CMOS circuits. and MOS transistor and circuit modeling.
		2	Explain and Analyze MOS static characteristics and interconnect effects.
		3	Demonstrate the design concepts of Combinational and Sequential MOS logic Circuits.
		4	Apply Combinational and Sequential MOS logic Circuits to build different Dynamic logic circuits
		5	Construct of Various CMOS Circuits using EDA Tools.



		1	Understand and apply the Verilog HDL
23VL5102	Digital VLSI Design	*	concepts for combinational logic.
		2	Understand and apply the Verilog HDL concepts for sequential logics
		3	Apply the synchronous design and ASM techniques in design of digital systems
		4	Analyze the reliabilty of digital systems by applying testing techniques
		5	Design of various digital systems by using EDA tools
	Analog IC Design	1	Application of the MOS transistors for the design of single stage amplifiers.
		2	Analysis and design of active & passive current Mirrors and the differential amplifiers with qualitative and quantative analysis.
23VL5103		3	Analyze the CMOS Op Amps, and various types of Op Amps with qualitative and quantative approaches.
End V had digital		4	Analyze the high frequency response of CS, CG and CD amplifiers and noise analysis of various amplifiers and analysis of non-linear analog circuits like switched capacitor circuits, PLL, ADC and DAC.
		5	Design and analysis of various MOS analog circuits using Cadence/ LT-SPICE environment for real time applications.
23EC5101 Artificial Intelligence Machine Learning	Artificial Intelligence & Machine Learning	1	Apply the possibilities offered by AI in finding solutions to domain-independent engineering problems and examine the fundamental blocks for building AI-based computer searches.
		2	Analyze machine learning approaches for clustering and classification by demonstrating architecture formulations, learning algorithms, and performance measurements.
		3	Analyze and reconfigure the dimensionality of datasets for training



			and interpret numerically.
		4	Apply optimization algorithms and estimate unknown phenomena.
		5	Experiment and design AI models on multiple datasets by providing discriminative analysis of the evaluation metrics.
23IE5149	Term Paper	1	The term paper has to be taken up by the MTech Second Semester students. It is based on independent research in one of the areas opted by the student. In a term paper, a student should demonstrate his/her ability in finding out the relevant sources, selection, an illustration of logic, and in organizing the information on the topic, gathering the data, processing, analyzing, and summarizing.
23UC5202 Algorithms For VLSI Design Automation		1	Apply the Algorithmic Graph Theory for the shortest path identification of the graph.
		2	Apply and analyze Placement, Floor planning and Routing with suitable algorithms
	3	Apply and realize the Physical Design cycle for FPGA's partitioning and routing for segmented and staggered models	
22VL5103	Low Power VLSi System Design	1	Understand the physics of power in CMOS circuits
		2	Analyses probabilistic power analysis and apply low power techniques at circuit level for CMOS circuits
		3	Apply low power techniques at gate level, architecture level and system levels
		4	Realize essential tasks in algorithm and architecture level low power design environments and Apply low power clock tree distribution techniques to create low power



			devices
		5	Experiment and design VLSI circuits with various low-power techniques using the Cadence VLSI design suite.
22VL5103 ASIC an	ASIC and FPGA Design	1	Understand the physics of power in CMOS circuits
		2	Analyses probabilistic power analysis and apply low power techniques at the circuit level for CMOS circuits
		3	Apply low power techniques at gate level, architecture level and system levels
		4	Realize essential tasks in algorithm and architecture level low power design environments.
		5	Experiment and design VLSI circuits with various low-power techniques using Cadence VLSI design suite.
22VL5503		1	Understand nanoelectronics and shrink-down approach
	Nano Electronics	2	Interpret the concept behind nano MOSFET and nanodevices
		3	Apply and Analyze the Schrodinger equation for different types of potentials in one dimension
		4	Understand the process of nanofabrication and characterization facilities
23VL5401	TESTING OF VLSI CIRCUITS	1	Understand the Testing Strategies of Digital Circuits and Fault Modeling Analysis.
		2	Interpret the Test Pattern for Testable Combinational & Sequential Circuits
		3	Apply Adhoc DFT Techniques, Scan Chain Design Rules and test pattern generation for BIST Architectures
		4	Apply the Faults in Digital Circuits and Memory Architectures



		5	Design and Analyze a Digital Circuit using testing methods
23Vl.51Q1	IC Fabrication Technology	1	Ability to understand the Concepts of design methodologies in routing and layout
		2	Understand different levels of modelling of digital circuits and scheduling
		3	Ability to understand the FPGA Technologies for development of physical design
		4	Analyze the routing and distribution of cells in ICs
23VL51Q2	System-on-Chip	1	Acquire knowledge about Top-down SoC design flow
		2	Understand the system level design of communication networks.
		3	Apply system level design and analyze MPSoC concepts
		4	Acquire knowledge about NoC
23VL51Q4	Semiconductor Device Modeling	1	Understand the basic device physics and study of MOS capacitor
		2	Understand and study of MOSFET physics and characteristics.
		3	Understanding the energy band diagrams of BJT and time dependent analysis.
		4	Understanding the concepts of designing of emitter, base and collector and study of modern BJT.

Academic Professor I/C

Dr. M. SUMAN
Professor & Head
Department of ECE
KLEF
Green Fields, Vaddeswaran.
Guntur Dist., A.P. PIN: 522 507