K L University

Department of ECE

Academic Year 2017

M.Tech Program VLSI

Mapping of ECE Department M.Tech (VLSI) Mission Statement with POs, PSOs and PEOs

Program Outcomes

Mission statement of K L University

Vision

To be a globally renowned university.

Mission

To impart quality higher education and to undertake research and extension with emphasis on application and innovation that cater to the emerging societal needs through all-round development of students of all sections enabling them to be globally competitive and socially responsible citizens with intrinsic values.

Vision and Mission statement of ECE department

VISION

- To evolve into a globally recognized department in the frontier areas of Electronics & Communication Engineering (ECE).

MISSION

M1- To produce graduates having professional excellence.

M2- To carry out quality research having social & industrial relevance.

M3- To provide technical support to budding entrepreneurs and existing

PROGRAM EDUCATIONAL OBJECTIVES (PEOS):

- **PEO1:** Employability in the diversified sectors of core industry, public sector or multinational corporations, in the domain of Semiconductor Technology, ASIC Design and Verification, Embedded Systems - Hardware and Software Development.
- **PEO2:** Ability to pursue higher education in technologies related to VLSI and Embedded Systems at institutes of repute and high standard leading to contributions to technology.
- **PEO3:** Attitude of lifelong learning and skills of effective inter-person communication resulting in leading diverse teams, with ethical and social behavior.

Programe Outcomes

PO1	a	Apply the knowledge of science, mathematics, and engineering principles for developing problem solving attitude.
PO2	b	Identify, formulate and solve engineering problems in the broad areas like System Design using VLSI and Embedded Platforms and tools, Semiconductor Technologies, Applications in Signal Processing, Machine Vision and Communication Networks.
PO3	c	Use different software tools in the domain of VLSI and Embedded Systems Design, Analysis and Verification such as Design entry, Synthesis, Functional and Timing Simulation, Floor-planning, Place and route, Layout editors, RTL schematic, Platform specific EDA sets, MATLAB.
PO4	d	Design and conduct experiments, analyze and interpret data, imbibe programming skills for development of simulation experiments.
PO5	e	Function as a member of a multidisciplinary team with sense of ethics, integrity and social responsibility.

Mapping of Mission statements with program educational objectives

	M1	M2	M3
PEO1	✓	✓	
PEO2		✓	✓
PEO3	✓		

Mapping of PEOs with Pos and PSOs

	PEO1	PEO2	PEO3
PO1	✓		
PO2	✓	✓	
PO3	✓		
PO4		✓	✓
PO5			✓

2017-18 (Semester I)									
S.NO	**COURSE CODE**	**COURSE NAME**	**Cos**	**COURSE OUTCOME**	**P01**	**PO2**	**PO3**	**PO4**	**PO5**
1	15 EC 5131	IC Fabricatio n	1	Abilitytounderstandthe Concepts of fabrication and steps following for fabrication	1				
			2	Understand different modelling technologies and materials used for fabrication		2			
			3	Ability to understand the concepts of lithography and deposition		2			
			4	Analyze the various etching technologies for preparation of ICs		2			
2	15EC5130	HDL & PLD Architectu res	1	Understand the basics concepts of digital system design, their modeling techniques in Verilog HDL.			1		
			2	Design of various Combinational & Sequential Logic realizations using Verilog HDL.			2		
			3	Compare and analysis of different PLD's and CPLD's architectures.			2		
			4	Memorize and analysis of different FPGA architectures.			2		
			5	Create and Analysis of digital modules through project oriented approach					3
3	15 EC 5128	MOS CIRCUIT DESIGN	1	Understand the basics concepts of digital system design, their modeling techniques in Verilog HDL.		1			
			2	Design of various Combinational &Sequential Logic realizations using Verilog HDL and design flow		2			
			3	Characteristics of inverter and calculation of different delays		2			
			4	Design of different combinational and sequential circuits		2			
			5	Create and Analysis of digital modules through project oriented approach					3
4	15 EC 5129	ALGORI THMS FOR	1	Ability to understand the Concepts of design methodologies in routing and layout	2				
			2	Understand different levels of modelling of digital circuits and scheduling	2				

		VLSI DESIGN	3	Ability to understand the FPGA Technologies for development of physical design				2	
			4	Analyze the routing and distribution of cells in ICs				2	
5	15 EC 51Q4	Nano Electronics	1	Ability to understand the Concepts nano Electronics	2				
			2	Understand different Architectures and equipment for nano electronics	2				
			3	Ability to understand the spintronics		2			
			4	Analyze the various memory devices and sensors in nano electronics		2			
6	15EC 51R3	Semiconductor Device Modeling	1	Understand the basics concepts of MOS transistors		2			
			2	Calculation of threshold voltage, delay, sensitivity		2			
			3	Characteristics Bipolar devices		2			
			4	Design of different combinational circuits		2			

Professor incharge

Head of the department