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Ref: KLEF/RO/ECE/CIRCULAR **Date:15-10-2018**

CIRCULAR

Sub: Organizing event "Seminar" for the students of Electronics and Communication Engineering, of Vaddeswaram Campus of KLEF – Reg.

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This is to inform that the Department of Electronics and Communication Engineering, KLEF, is Organizing a "Seminar on Low Power VLSI Design Strategies: Trends and Challenges" for the students of Electronics and communication Engineering, Vaddeswaram Campus of KLEF on, 18-10-2018, as details below:

Event Name: "Workshop"
Date: 18-10-2018
Venue: R-106

All the students of ECE, are invited to attend this program.
Dy-HOD's & Year coordinators are requested to bring this information to the attention of all ECE students and encourage them to participate in this program.

HOD, ECE

Professor & Alternate HOD
Department of ECE
K L University
VADDESWARAM
Guntur Dt., A.P., India.

To
All ECE Students,
All ECE Faculty,
Principal.

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A Seminar On "Low Power VLSI Design Strategies: Trends and Challenges"

By

Always@VLSI

Department Of ECE

Name of the event: Low Power VLSI Design Strategies: Trends and Challenges

Dates:18-10-2018

Venue:R106

No. of students participated: 39

Objective of the event:

The objectives of the Seminar "Low Power VLSI Design Strategies: Trends and Challenges" are designed to provide participants with a comprehensive understanding of low power VLSI design principles, emerging trends, and the challenges associated with designing energy-efficient integrated circuits. The specific objectives include:

Understanding Low Power Design Fundamentals: Provide participants with a solid foundation in the fundamental principles of low power VLSI design, including power consumption metrics, power management techniques, and energy-efficient design methodologies.Exploration of Power Reduction Techniques: Introduce participants to a variety of power reduction techniques, including voltage scaling, clock gating, power gating, and dynamic power management, and discuss their implementation strategies and trade-offs.Overview of Low Power Design Tools and Methodologies: Familiarize participants with the latest simulation tools, design methodologies, and optimization techniques used in low power VLSI design, enabling them to effectively analyze, optimize, and validate low power circuits.

Integration of Low Power Techniques: Demonstrate how to integrate low power design techniques into various stages of the VLSI design flow, including architecture design, circuit design, and physical design, to achieve significant power savings without compromising performance.Analysis of Power Consumption: Teach participants how to accurately estimate, measure, and analyze power consumption in VLSI circuits using simulation tools, power profiling techniques, and hardware monitoring instruments.Exploration of Advanced Low Power Design Concepts: Discuss emerging trends and advanced concepts in low power VLSI design, such as near-threshold computing, energy harvesting, and power-aware design for Internet of Things (IoT) devices, enabling participants to stay abreast of cutting-edge developments in the field.Identification and Mitigation of Design Challenges: Address common challenges and limitations associated with low power VLSI design, such as timing closure issues, increased design complexity, and reliability concerns, and provide strategies for overcoming these challenges effectively.

Case Studies and Best Practices: Present real-world case studies and industry best practices in low power VLSI design, allowing participants to gain practical insights into successful low power design implementations and learn from real-world examples.Interactive Seminars and Hands-on Exercises: Provide participants with opportunities for hands-on experience through interactive Seminars, design challenges, and practical exercises focused on low power VLSI design, reinforcing key concepts and enhancing their problem-solving skills.Overall, the Seminar aims to empower participants with the knowledge, skills, and tools necessary to address the growing demand for energy-efficient integrated circuits in various applications, ranging from portable devices and IoT sensors to high-performance computing systems. By mastering low power VLSI design strategies, participants will be equipped to develop innovative, power-efficient solutions that meet the evolving needs of the semiconductor industry.

Description of the event:

The Seminar "Low Power VLSI Design Strategies: Trends and Challenges" is an intensive program designed to explore the latest techniques, trends, and challenges in designing energy-efficient Very Large Scale Integration (VLSI) circuits. In today's increasingly mobile and battery-powered world, low power design has become a critical aspect of VLSI engineering. This Seminar provides participants with the knowledge and tools necessary to tackle the complexities of low power VLSI design effectively.

Throughout the Seminar, participants will engage in a series of interactive sessions, lectures, case studies, and hands-on exercises led by industry experts and experienced practitioners. The Seminar will cover a wide range of topics, including fundamental principles, advanced techniques, emerging trends, and practical challenges in low power VLSI design.Key components of the Seminar include:

Fundamentals of Low Power Design: Participants will gain a solid understanding of the fundamental principles of low power VLSI design, including power consumption metrics, power management techniques, and energy-efficient design methodologies.Power Reduction Techniques: An exploration of various power reduction techniques, such as voltage scaling, clock gating, power gating, and dynamic power management, will be conducted, along with discussions on their implementation strategies and trade-offs.Tools and Methodologies: Familiarization with the latest simulation tools, design methodologies, and optimization techniques used in low power VLSI design will be provided, enabling participants to effectively analyze, optimize, and validate low power circuits.

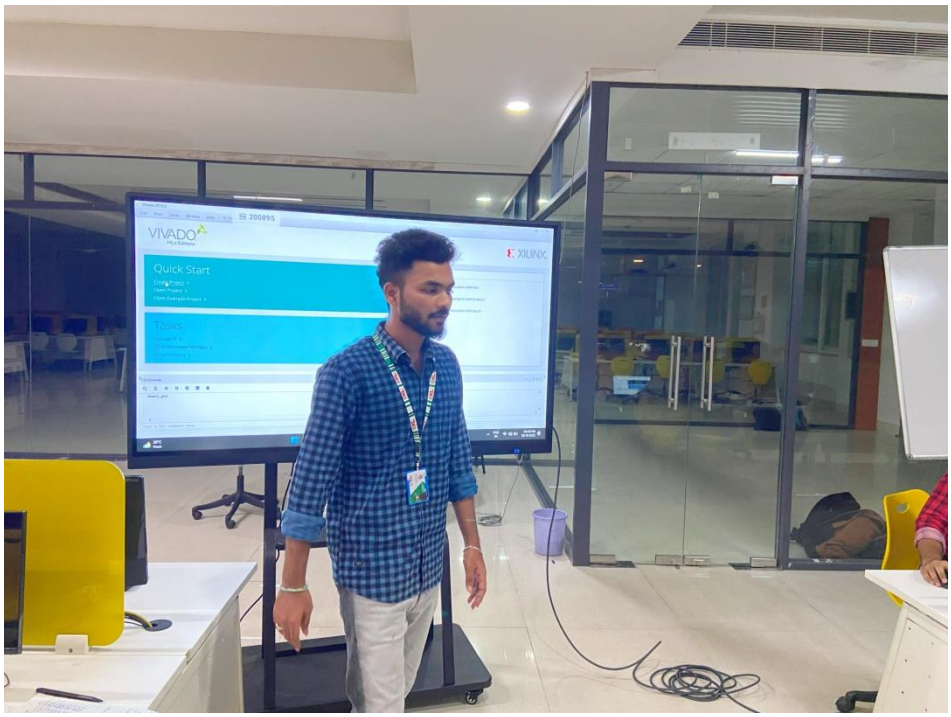
Integration of Low Power Techniques: Participants will learn how to integrate low power design techniques into different stages of the VLSI design flow, from architecture design to physical design, to achieve significant power savings without compromising performance.Advanced Concepts and Emerging Trends: Discussion on emerging trends and advanced concepts in low power VLSI design, such as near-threshold computing, energy harvesting, and power-aware design for Internet of Things (IoT) devices, will be conducted to keep participants informed about cutting-edge developments in the field.Challenges and Solutions: Addressing common challenges and limitations associated with low power VLSI design, such as timing closure issues, increased design complexity, and reliability concerns, will be an integral part of the Seminar, with strategies for overcoming these challenges effectively.Hands-on Exercises: Participants will have the opportunity to apply their knowledge through hands-on exercises, design challenges, and practical simulations focused on low power VLSI design, reinforcing key concepts and enhancing their problem-solving skills.

Outcome of the event:

Overall, the outcome of the Seminar will be participants who are well-equipped with the knowledge, skills, and tools necessary to excel in low power VLSI design, contributing to the

development of innovative, energy-efficient integrated circuits that drive technological advancements and meet the needs of a sustainable future.

Photos of the event:



Students participating in low power design seminar.

Participant's List:

S.NO	ID.NO	NAME	BRANCH	SIGNATURE
1.	160041035	JADDU JAYASAI KISHORE	ECE	
2.	160041022	GORRIPATI DIVYA SAI TEJA	ECE	
3.	160041019	KIRIGADALA RUDREGOWDA	ECE	
4.	160041017	VINJAMURI PAVAN KUMAR	ECE	
5.	160041010	KOLLIPARA SAI SREE ROHINI	ECE	
6.	160041008	KANKANAMPATI MANISHA	ECE	
7.	160041006	JANGA SATYA RISHI TEJA	ECE	
8.	160040996	KONAKALLA GEETHA SREE	ECE	
9.	160040989	YEDDULA JITENDRA REDDY	ECE	
10.	160040976	YADAVALLI SUNDAR SAI	ECE	
11.	160040963	VENKATA SAI AJAY	ECE	
12.	160040948	VELLATURI VENKATA	ECE	
13.	160040947	VENKATA PRUDHVI	ECE	
14.	160040939	VEERA LOHIT K	ECE	
15.	160040925	SIVA PRUDHVISH VALIVETI	ECE	
16.	160040922	VALE TARUN KUMAR	ECE	
17.	160040921	VAKALAPUDI SAI RAJESH	ECE	
18.	160040920	VADLAMUDI VENKATA	ECE	
19.	160040916	VADDEVALLI PAVAN	ECE	
20.	160040910	KOTI REDDY UPPELA	ECE	
21.	160040909	UPPALAPATI CHANDU	ECE	
22.	160040904	T. TUMPUDI NIKHILESH	ECE	
23.	160040895	Q. THUMMURU	ECE	
24.	160040894	C. PRASANTH KUMAR REDDY	ECE	
25.	160040891	MADHUSUDHAN	ECE	
26.	160040890	ABHISHEK THOTAKURA	ECE	
27.	160040885	THOPURI CHANAKYA	ECE	
28.	160040884	THOMMANDRU JAYARAM	ECE	
29.	160040883	THIRUMALASETTY BALAJI	ECE	
30.	160040859	SURI KAVYA	ECE	
31.	160040858	NARENDRA SURARAPU	ECE	
32.	160040854	SUNKAVALLI SURYA TEJA	ECE	
33.	160040850	N. SUDINEEDI VENKATA	ECE	
34.	160040841	SOMU VENKATASAINIKHIL	ECE	
35.	160040840	SOMIREDDY JAYA SAI SRI	ECE	
36.	160040830	SHAKAMURI MEGHANA	ECE	
37.	160040829	SHAIK YASWANTH BASHA	ECE	
38.	160041058	KANNEGANTI PAVAN	ECE	
39.	160040975	YACHAMANENI TANMAYEE	ECE	

In charge
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