

WORKSHOP REPORT

One-Day Online Workshop on Technical Session on Synopsys Semiconductor Design and Simulation Solutions Covering EDA, TCAD (Sentaurus), and Atomistic Materials Modeling (QuantumATK)

1. Event Overview

Event Title: Technical Session on Synopsys Semiconductor Design and Simulation Solutions covering EDA, TCAD (Sentaurus), and Atomistic Materials Modeling (QuantumATK)

Workshop Type: One-Day Workshop (Online)

Date: 10 July 2026

Time: 10:00 AM onwards

Mode: Online

Organized By: Department of ECE, in association with Academic Staff College (ASC), KLEF, Vijayawada

2. Workshop Coordinators

- Dr. Chella Santhosh – Associate Professor, Dept. of ECE
- Dr. S. Vamsee Krishna – Assistant Professor, Dept. of ECE

3. Session Schedule and Speakers

S.No.	Session Title	Speaker	Time
1	Advanced Semiconductor Material and Device Modeling with Synopsys QuantumATK Software	Er. Deepak Upadhyay, Principal Application Engineer, Integrated Microsystem	10:00 AM – 12:00 PM
2	Advanced Semiconductor Process and Device Simulation with Synopsys Sentaurus TCAD	Er. Sachin Yadav, Application Engineer, Integrated Microsystem	2:00 PM – 3:00 PM
3	Technical Session on Synopsys Electronic Design Automation (EDA) Solutions	Mr. Atul Kumar Srivastava, Application Engineer, Integrated Microsystem	4:00 PM – 5:00 PM

4. About the Sessions

Session 1: Advanced Semiconductor Material and Device Modeling with Synopsys QuantumATK Software

This session, led by Er. Deepak Upadhyay, focused on atomistic-level modeling of semiconductor materials and devices using Synopsys QuantumATK, covering simulation techniques used for exploring novel materials and next-generation device structures.

Session 2: Advanced Semiconductor Process and Device Simulation with Synopsys Sentaurus TCAD

Delivered by Er. Sachin Yadav, this session covered Technology Computer-Aided Design (TCAD) using the Synopsys Sentaurus platform, addressing semiconductor process and device-level simulation methodologies.

Session 3: Technical Session on Synopsys Electronic Design Automation (EDA) Solutions

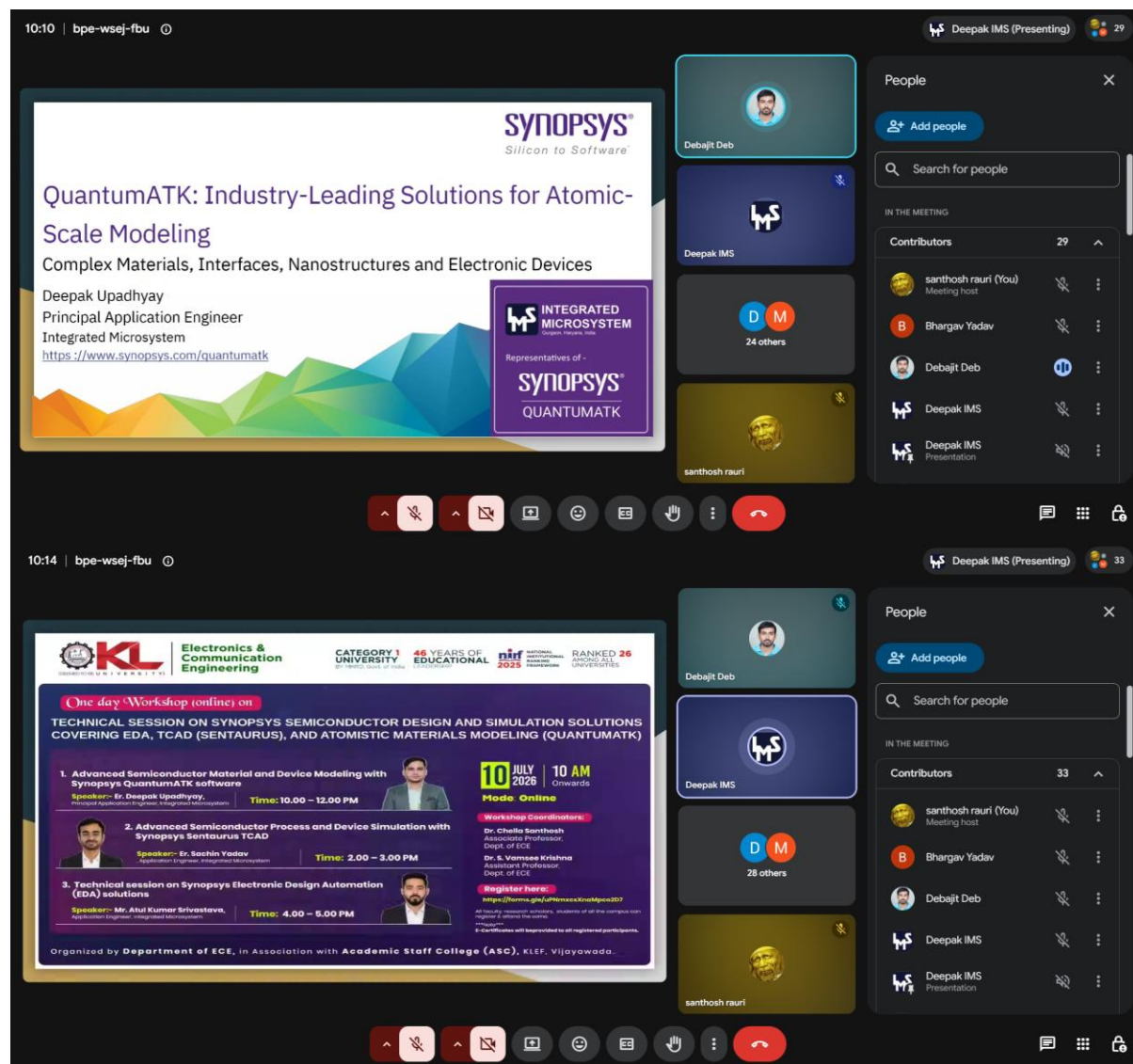
Presented by Mr. Atul Kumar Srivastava, this session introduced participants to Synopsys' Electronic Design Automation (EDA) tools and their applications in semiconductor design workflows.

5. Registration and Certification

All faculty, research scholars, and students across all campuses were eligible to register and attend the workshop.

Registration Link: <https://forms.gle/uPNmxcsXnaMpc02D7>

E-Certificates were provided to all registered participants.



The screenshot shows a Zoom meeting interface. The main window displays a presentation slide titled "QuantumATK: Industry-Leading Solutions for Atomic-Scale Modeling" by Deepak Upadhyay, Principal Application Engineer at Integrated Microsystem. The slide includes the Synopsys logo and a link to the QuantumATK website. The right sidebar shows a list of participants, including Debajit Deb, Deepak IMS, and santhosh rauri. The bottom of the screen shows the Zoom controls and a list of contributors.

QuantumATK: Industry-Leading Solutions for Atomic-Scale Modeling
Complex Materials, Interfaces, Nanostructures and Electronic Devices
Deepak Upadhyay
Principal Application Engineer
Integrated Microsystem
<https://www.synopsys.com/quantumatk>

One day Workshop (online) on:
TECHNICAL SESSION ON SYNOPSYS SEMICONDUCTOR DESIGN AND SIMULATION SOLUTIONS COVERING EDA, TCAD (SENTAURUS), AND ATOMISTIC MATERIALS MODELING (QUANTUMATK)

1. Advanced Semiconductor Material and Device Modeling with Synopsys QuantumATK software
Speaker:- Er. Deepak Upadhyay, Principal Application Engineer, Integrated Microsystem. Time: 10.00 – 12.00 PM

2. Advanced Semiconductor Process and Device Simulation with Synopsys Sentaurus TCAD
Speaker:- Er. Sachin Yadav, Application Engineer, Integrated Microsystem. Time: 2.00 – 3.00 PM

3. Technical session on Synopsys Electronic Design Automation (EDA) solutions
Speaker:- Mr. Atul Kumar Srivastava, Application Engineer, Integrated Microsystem. Time: 4.00 – 5.00 PM

Workshop coordinators:-
Dr. Chaito Santhosh, Associate Professor, Dept. of ECE
Dr. S. Vamshee Krishna, Assistant Professor, Dept. of ECE

Register here:-
<https://forms.gle/uPNmxcsXnaMpc02D7>

All faculty, research scholars, students of all the campus can register & attend the session.
E-Certificates will be provided to all registered participants.

Organized by Department of ECE, in Association with Academic Staff College (ASC), KLEF, Vijayawada...

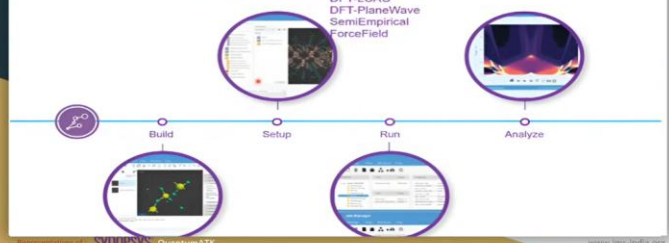
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Deepak IMS (Presenting)

Simulation Software for Nanoscience Professionals

QuantumATK Platform for Atomic-Scale Modeling

DFT-LCAO
DFT-PlaneWave
Semi-Empirical
ForceField



Debjit Deb

Deepak IMS

37 others

santhosh rauri

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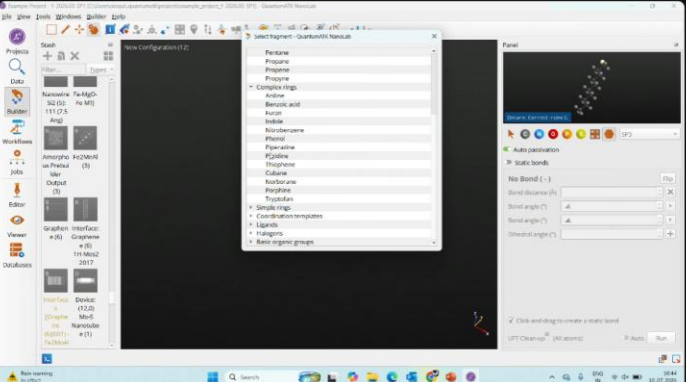
IN THE MEETING

Contributors 42

- santhosh rauri (You) Meeting host
- Ayush Mamoriya
- Bhargav Yadav
- Debjit Deb
- Deblu Sahu

10:44 | bpe-wsej-fbu

Deepak IMS (Presenting)



Debjit Deb

Deepak IMS

42 others

santhosh rauri

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IN THE MEETING

Contributors 46

- santhosh rauri (You) Meeting host
- Ayush Mamoriya
- bharathreenivasulu vak...
- Bhargav Yadav
- Debjit Deb

10:16 Fri, 10 Jul
35
93

What is QuantumATK?

QuantumATK is an *integrated platform of electronic and atomic-scale modeling tools* developed by expert software engineers and scientists to meet the highest requirements of usability and efficiency.



Core Simulation Engines



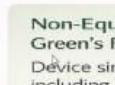
Density Functional Theory
Accurate electronic structure calculations



Semi-Empirical Tight Binding



Classical and Machine-Learned Force Fields
Versatile interatomic



Non-Equilibrium Green's Functions
Device simulations including electron transport

Complete Solution for Materials Modeling

Fully integrated platform with seamless multi-method integration.

- Access diverse atomistic methods implemented and fully integrated in a single platform
- Density Functional Theory
- Semi-Empirical Tight Binding
- Force Fields (CL, ML)
- Non-Equilibrium Green's Functions

Full Support

- Expert Guidance
- Personalized Solutions
- Fast Response Times



www.ims-india.org

Deepak is presenting



You



Deepak



Debjit



M



santhosh



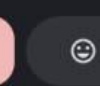
Dr.Purva Sharma



Rooban

27 others











10:16 Fri, 10 Jul
35



What is QuantumATK?
QuantumATK is an integrated platform of electronic and atomic scale modeling tools developed by expert software engineers and scientists to meet the highest requirements of usability and efficiency.

Core Simulation Engines

- Density Functional Theory: Accurate electronic structure calculations
- Semi-Empirical Tight Binding: Classical and Machine-Learned Force Fields, Quantum Mechanics
- Non-Equilibrium Green's Functions: Accurate simulations involving electron transport

Complete Solution for Materials Modeling
Fully integrated platform with seamless multi-method integration

- Accurate electronic structure calculations
- Density Functional Theory
- Semi-Empirical Tight Binding
- Force Fields (DFT, ML)
- Non-Equilibrium Green's Functions

Full Support

- Expert Guidance
- Personalized Solutions
- Real-Response Training

Deepak is presenting


Deepak


Debajit


Dr. Purva


You


santhosh


M

28 others

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People Information Tools

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In call


rajitha korrapati (You)


santhosh rauri
Meeting host


Bhargav Yadav


Debajit Deb


Deepak IMS


Deepak IMS


Deepak IMS (Presenting)


Dr. Nvk Ramesh


Dr. Pratap Kumar Das


Dr. Srinivasarao Alluri


Dr. A. Kiran Kumar


Dr. J. Lakshmi Prasanna

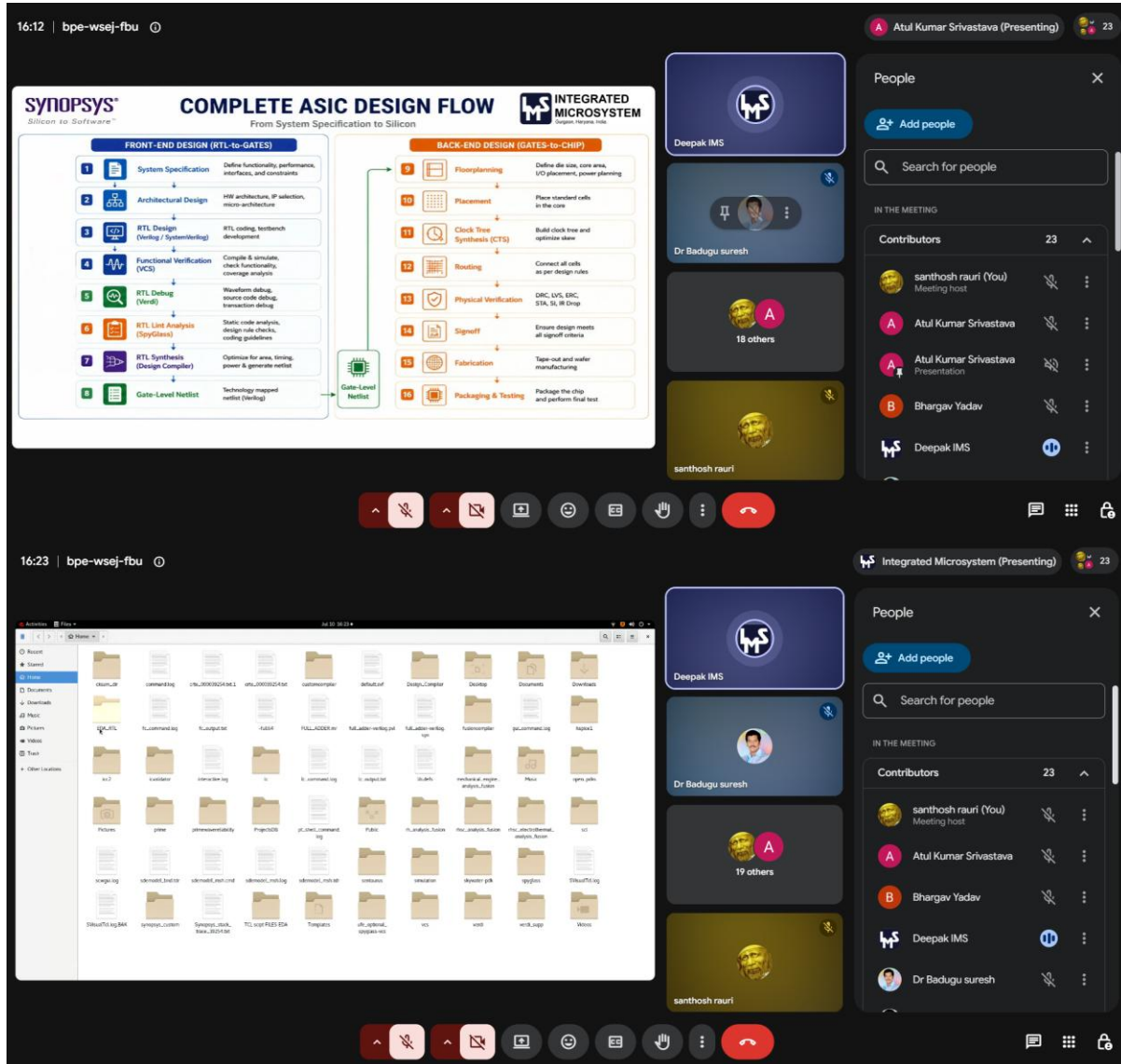

Dr. Purva Sharma


G L P ASHOK


Ghali venkata subbarao


gousya sk

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16:23 | bpe-wsej-fbu

SYNOPSYS[®] COMPLETE ASIC DESIGN FLOW

From System Specification to Silicon

FRONT-END DESIGN (RTL-to-GATES)

- 1 System Specification: Define functionality, performance, interfaces, and constraints.
- 2 Architectural Design: HW architecture, IP selection, micro-architecture.
- 3 RTL Design (Verilog / SystemVerilog): RTL coding, testbench development.
- 4 Functional Verification (VCS): Compile & simulate, check functionality, coverage analysis.
- 5 RTL Debug (Verdi): Waveform debug, source code debug, interaction debug.
- 6 RTL Lint Analysis (SpyGlass): Static code analysis, design rule checks, coding guidelines.
- 7 RTL Synthesis (Design Compiler): Optimize for area, timing, power & generate netlist.
- 8 Gate-Level Netlist: Technology mapped netlist (Netlist).

BACK-END DESIGN (GATES-to-CHIP)

- 9 Floorplanning: Define die size, core area, I/O placement, power planning.
- 10 Placement: Place standard cells in the core.
- 11 Clock Tree Synthesis (CTS): Build clock tree and optimize skew.
- 12 Routing: Connect all cells as per design rules.
- 13 Physical Verification: DRC, LVS, ERC, STA, SI, IR Drop.
- 14 Signoff: Ensure design meets all signoff criteria.
- 15 Fabrication: Tape-out and wafer manufacturing.
- 16 Packaging & Testing: Package the chip and perform final test.

Integrated Microsystem (Presenting)

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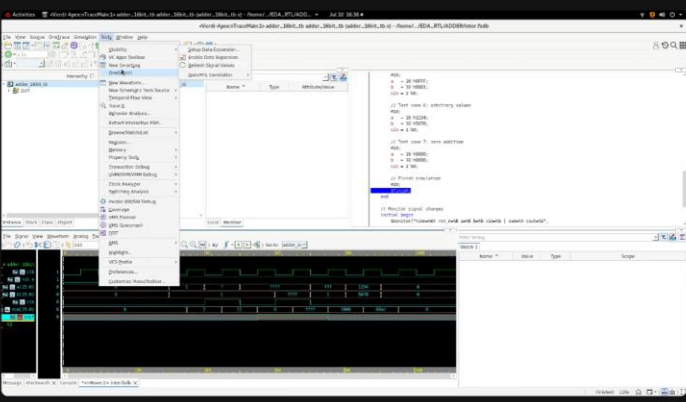
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Contributors 23

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- Atul Kumar Srivastava
- Bhargav Yadav
- Deepak IMS

16:36 | bpe-wsej-fbu



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23

Deepak IMS

Dr Badugu suresh

19 others

santhosh rauri

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18

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Dr Badugu suresh

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Atul Kumar Srivastava Presentation

Bhargav Yadav

Deepak IMS

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6. Summary

The workshop offered a comprehensive, single-day overview of the Synopsys semiconductor design and simulation ecosystem, spanning three complementary levels of the semiconductor design flow: atomistic materials and device modeling (QuantumATK), process and device-level simulation (Sentaurus TCAD), and circuit/system-level Electronic Design Automation (EDA) tools. Conducted online and coordinated by the Department of ECE in association with the Academic Staff College, the event was open to faculty, research scholars, and students across all campuses, with e-certificates issued to registered participants.

Co-ordinator
Dr. Chella Santhosh

HOD
Dr. I Govardhani