K L UNIVERSITY

DEPARTMENT OF ELECTRONICS & COMPUTER ENGINEERING

A REPORT

ON

TWO DAY WORKSHOP ON

"DIGITAL SYSTEM DESIGN AND VERIFICATION USING SYSTEM VERILOG"

Organized by

Embedded System & Sensor Networks Research Group

&

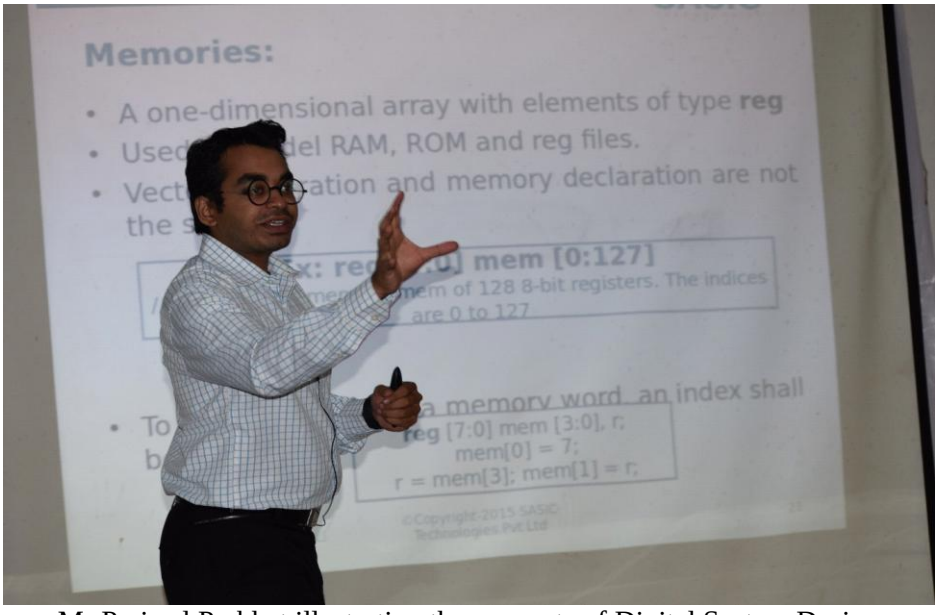
Department of Electronics & Computer Engineering

In Association With

Koneru Chapter IETE-KLUSF

Date: 17th & 18th march, 2016 **Venue**: C121

Department of Electronics & Computer Engineering of K L University organized a two day workshop on "**DIGITAL SYSTEM DESIGN AND VERIFICATION USING SYSTEM VERILOG**" on 17th and 18th march, 2016 in association with Sasic technologies pvt ltd ,IETE KLUSF and CSI-Koneru Chapter.Mr. Prajwal prabhat, Mr.Avinash, Mr.sreehari from Sasic technologies was the resource persons for the workshop.



Mr.Prajwal Prabhat illustrating the concepts of Digital System Design

Mr. Prajwal prabhat is a senior design verification engineer presently working in SASIC TECHNOLOGIES private limited. Mr.prajwal prabhat has an overall experience of 5 years in VLSI and 6 years in professional experience, he has knowledge on various tools like modelsim, vcs, git, perforce and many more. The convener of the workshop is Mr.M.Venkateswa Rao.

Faculty and Student participation in the workshop

The students of B.Tech/M.Tech- ECM, ECE, EEE, CSE attended the workshop.

Day 1 (17th march, 2016)

The first day of the workshop started at 9.30 a.m. with a Welcome note by P.spandana and K.Rishitha and Later on Brief introduction was given by Dr.T.Anuradha Alt HOD-ECM

Dr.T.Anuradha –AHOD –addressing the gathering

Mr. Prabhat started the session at 10:00 a.m. with the Introduction of VLSI and following topics

- Fundamentals of Processor Design
- Challenges of RTL Design in VLSI.
- IC/Soc design flow
- Introduction to Hdls
- Lexical tokens
- Advanced test bench concepts and strategies

- system Verilog Basics
- complete system Verilog test bench

The afternoon session of the workshop focused on the level of abstraction which defines VHDL – defined using various levels of abstraction. And different levels of modelling techniques were discussed

- switch level modelling
- gate level modelling
- data flow modelling
- behavioural modelling

Mr. Prajwal prabhat elaborating the importance of system Verilog.

Day 2 (18th march, 2016)

The morning session of second day of workshop was started at 9:00am in the morning. The session was started with the hands on experience on theory explanation of HDL- all other behaviour statements appear only inside these structured, procedural constraints. Also discussed about 3 pillars of verilog:

- assign state ,always ,initiation [named boards]

Loop constraints: forever loop

Syntax: forever procedural statement continuously

System tasks: To handle simple I/O and various function during simulation.

$ Display , $ write, $ monitor , $ Strobe


Practical Sessions on System Verilog

After a small break, the session was continued with the verification challenge: more theoretical values, Functional verification: design accurately performs the tasks independently by the overall system architecture

- To detect missing feature.
- To detect missing corner.

Also, a simple program to control a HDL was explained.

The afternoon session was again a hands on experience with the modes in win

- Command mode –cmd
- Visual mode
- Insert mode

"I" or "insert" on keyboard. 'Esc' to cmd mode.

Paste line –"p"

And the discussion continued on Verilog represented a tremendous productivity improvement for circuit designers who were already using graphical schematic capture software and specially written software programs to document and simulate electronic circuits.

CO-CONVENER	**CONVENER**	**HOD-ECM**
Mr.M.Venkateswarao	Mr.T.Narendra babu	Dr K.Raghava rao.