KL UNIVERISTY
FIRST SEMESTER 2010-11
Course Handout
Academic Division

Dated: 07-07-2010

Course No. **: EM C201**
Course Title **: Switching Theory & Logic Design**
Course Structure **: 3-0-0**
Course coordinator **: Dr S Balaji**
Instructors **:M Vidya Sri**

1. Course Description:

Boolean Algebra, Postulates and theorems, Minimization of Switching functions, Karnaugh map method, Tabulation method, Logic gates, Binary Adders, Carry look ahead Adder, Decoders, Encoders, Multiplexer, De-multiplexer, Sequential circuit models, Flip Flops, Mealy Moore Models, Registers, Counters, RAM, PAL,PLA.

2. Scope and Objective of the Course:

This course aims to teach a set of skills necessary to design digital circuits.

The Course Objectives is to
(1) Learn about various methods of designing and construction of systems such as digital computers, data communication, digital recording and many other applications that require digital hardware.
(2) Distinguish the benefits of continues and discrete networks.
(3) Able to design various synchronous & Asynchronous counters.
(4) To identify suitable designing procedures for the given problems.

The Study of Switching theory and Logic Design involves 2 complementary Goals.

The 1st Goal is to learn Basic tools for the design of digital circuits and fundamental concepts used in the design of digital systems.
The 2nd Goal is to realize logic networks, digital computers with special attraction given to 3 basic structures of programmable logic devices. PROM, PLA, PAL devices.
After Completing this course student should be able to know how to design combinational logic circuits, sequential logic circuits and memories

3. Books:

(i) Textbook:

a. M.Morris Mano,'Digital Design', 3rd Edition, PHI.
b. Donald D.Givone ,'Digital principles and Design', TMH.

(ii) Reference Book:

a. A Anand Kumar,'Fundamentals of Digital Circuits' PHI,
b. Kohavi ZVI,'Switching and Finite Automata Theory', 2nd Edition, TMH
c. RP Jain 'Modern Digital Electronics', 2nd Edition, TMH

4. Syllabus:

UNIT-I

BOOLEAN ALGEBERA: Axiomatic definition of Boolean algebra. Binary operation. Postulates and theorems, Switching functions, Canonical forms and standard forms, Simplification of switching functions using theorems. Minimization of switching functions: Karnaugh map method, Quine McCluskey tabular method, Prime implicants and essential prime implicants.

UNIT-II

COMBINATIONAL LOGIC DESIGN: Single output and multiple-output combinational logic circuit design, AND-OR, OR-AND and NAND/NOR relations, exclusive-OR and Equivalence functions. Binary Adders, Carry look ahead Adder, magnitude comparator, sub tractors. LOGIC DESIGN WITH MSI COMPONENTS: Decoders, Encoders, Priority Encoders, Multiplexer, De-multiplexer, Parity generator – checker, Code converters

UNIT-III

SEQUENTIAL LOGIC DESIGN: Classification of sequential circuits, sequential circuit model, latches, flip-flops, and excitation table, characteristic equation, state diagram, Mealy & Moore Models, sequence detectors, Analysis of clocked Sequential Circuits.

UNIT-IV

REGISTERS AND COUNTERS: Registers, Shift Register, Ripple Counters, Synchronous Counters.

UNIT V

Memory and Programmable logic: Random Access Memory, Read only memory, Programmable logic Array, Programmable Array Logic**.**

5.Course Plan:

Course plan is meant as a guideline. There may probably be changes.

Lecture No.	Learning Objectives	Topics to be Covered	Chapter in the text book
1	Logic operations for two variables	Boolean algebra	T1,P33
2	Logic operations for two variables	Boolean algebra	T1,P33
3	Theorems and properties	Postulates and theorems	T1,P37
4	Theorems and properties	Postulates and theorems	T1,P39
5	Boolean Functions	Switching functions	T1,P45
6	MinTerms and Max Terms	Canonical forms and standard forms	T1,P45
7	Sum Of Max terms and Product of Min terms	Canonical forms and standard forms	T1, P47
8	Theorems and Properties	Simplification of switching functions using theorems	T2,P345
9	Theorems and Properties	Simplification of switching functions using theorems	T2,P346

10	Two, Four & Five variable map	Karnaugh map method	T1,P65
11	SOP & POS	Karnaugh map method	T1,P67
12	Prime Implicants & don't care conditions	Karnaugh map method	T1,P81
13	Prime Implicants	Quine McCluskey tabular method	T2,P166
14	Algorithms for generating Prime implicants	Quine McCluskey tabular method	T2,P167
15	Irredundant Expressions & Conjunctive Normal Formulas	Prime implicants and essential prime implicants.	T2,P178
16	Basic Components used in design	combinational logic circuit design	T1,P111
17	Basic Components used in design	combinational logic circuit design	T1,P115
18	Two Level Circuits	AND-OR, OR-AND and NAND/NOR relations	T2,P92
19	Two Level Circuits	exclusive-OR and Equivalence functions	T2,P92
20	Design of Combinational Circuits	Binary Adders	T1, P119
21	Design of Combinational Circuits	Carry look ahead Adder	T2,P236
22	Design of Combinational Circuits	Magnitude comparator, sub tractors	T1,P113
23	Conversion of Information	Encoders, Priority Encoders	T1,P139
24	Conversion of Information	Decoders	T1,P134
25	Signal Compression	Multiplexer, De-multiplexer	T2,P262
26	Error Correcting and Verification	Parity generator – checker,	T1,P97
27	Conversion of codes	Code converters	T1,P450
28	Design of sequential circuits	Classification of sequential circuits	T1,P167
29	Models of Synchronous sequential circuit	sequential circuits model	T1,P168
30	Two state Circuit	Latches	T1,P169
31	Feedback Property	Flip-flops	T1,P172
32	Inputs to change states	Flip-flops	T1,P175
33	Inputs to change states	Flip-flops	T1,P179
34	State Models	Mealy & Moore Models	T1,P189
35	State Models	Mealy & Moore Models	T1,P190
36	State Diagram design example	Sequence detectors, Analysis of clocked Sequential Circuits.	T1,P180
37	Group of Flip flops	Registers	T1,P217
38	Shift Right & Shift Left	Shift Register	T1,P219
39	Asynchronous Counters	Ripple Counters	T1,P227

40	Modulus Design	Synchronous Counters.	T1,P232
41	Modulus Design	Synchronous Counters	T1,P235
42	Design of Memories	RAM&ROM	T1,P256
43	Logic Array Design	PLA	T1,P276
44	Array Logic Design	PAL	T1,P280
45	Array Logic Design	PAL	T1,P282

6.Self learning material:

Unit	Topic	Source
I	Binary Operations	Fundamentals of logic Design, Charles H.Roth,Jr.
III	Introduction to Combinational & Sequential circuits	Digital Circuits& Logic Design, Samuel C.Lee
III	Conversion of Flip Flops	Digital Logic Design, A.Anand Kumar
IV	Ring Counter & Johnson Counter	Digital Design',3rd Edition, M.Morris Mano
V	Complex Programmable Logic Devices	Fundamentals of logic Design, Charles H.Roth,Jr.

7.Evaluation Scheme:

Component	Duration (minutes)	% Weightage	Marks	Date & Time	Venue
Test-1	50 Min	10	10	10-08-2010 9.30 to 10.20 A.M	CSE103,202, 209,309
Test-2	50 Min	10	10	14-09-2010 9.30 to 10.20 A.M	CSE103,202, 209,309
Assignement submission		5	5	Continuous	
Assignment Test	50 Min	5	5	26-10-2010 9.00 to 10.20 A.M	CSE103,202, 209,309
Quiz	30 Min	5	5	26-10-2010 9.00 to 10.20 A.M	CSE103,202, 209,309
Regular Lab Evaluation	Continuous	0	0		
Comprehensive Lab Exam	3 Hrs	0	0		
Comprehensive Exam	3 Hrs	60	60		
Attendance for Theory & Tutorial		5	5	Continuous	
Attendance for Lab		0	0	Continuous	

8. Chamber consultation hour: Informed in the class in first week.

9. Notices: All notices regarding the course will be put in E-learning website.

Course Coordinator