



Academic
Staff College

Recent Trends in VLSI Chip/ Devices for Sensor Applications

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Conducting 2 weeks AICTE-ATAL Faculty Development Program on “Recent trends in VLSI Chip devices/Circuits for Sensor Applications” by Microelectronics & VLSI Research Group, Department of ECE, KLEF – Reg.

Registrar <registrar@kluniversity.in>

Thu 9/8/2022 11:13 AM

To:VARADA VENKATA SUBBARAO <subbarao6373@kluniversity.in>;BRAJESH KUMAR SHUKLA <brajesh.shukla@kluniversity.in>; NAWEEN KUMAR <naween@kluniversity.in>;GARIGIPATI RAMA KRISHNA <umarkcse@kluniversity.in>;NAGALAKSHMI THIRUNAVUKKARASU <lakshmisenthil@kluniversity.in>;DODDI SURESH KUMAR <sureshdkumarmca@kluniversity.in>; GARIKIPATI NAGA LAKSHMI SOWJANYA <chlks1709@kluniversity.in>;AREPALLI GOPI <gopi.arepalli@kluniversity.in>; anushaponnuru588@kluniversity.in <anushaponnuru588@kluniversity.in>;SRITHAR.S <sss.srithar@kluniversity.in>;SREEDHAR BURADA <sreedharburada@kluniversity.in>;drsatishtatavarthi@kluniversity.in <drsatishtatavarthi@kluniversity.in>;Yogesh Tripathi <yogeshtripathi27@kluniversity.in>;asesh.trpathy@kluniversity.in <asesh.trpathy@kluniversity.in>;Dr. Iwin Thanakumar Joseph. S <iwineee2006@kluniversity.in>;SaiRam Vakkalanka <sairam.vakkalanka@kluniversity.in>;Anjana Devi A <anjana.nadam@kluniversity.in>;Sai Durga Tejaswi <saidurga.vinna@kluniversity.in>;Raj Kumar Parida <rajkumarparida@kluniversity.in>;CH Divya <chdivya333@kluniversity.in>

📎 1 attachments (1 MB)

AICTE-ATAL FDP Poster.jpg;

Ref: KLEF/RO/ECE/2022-23

Date: 08-09-2022

Orders of the Vice Chancellor dt.08.09.2022

CIRCULAR

Sub: Conducting 2 weeks AICTE-ATAL Faculty Development Program on “**Recent trends in VLSI Chip devices/Circuits for Sensor Applications**” by Microelectronics & VLSI Research Group, Department of ECE, KLEF – Reg.

Ref: Letter dated 05.09.2022 from Dr.K. Srinivasa Rao, Research Group Head, ECE, forwarded by Dr.M. Suman, HoD-ECE.

This is to inform that Microelectronics & VLSI Research Group, Department of ECE, KLEF, is conducting two weeks AICTE-ATAL Faculty Development Program on “**Recent trends in VLSI Chip devices/Circuits for Sensor Applications**” , for faculty members, research scholars and students, as per the details given below.

Dates : 26.09.2022 to 01.10.2022 in online mode
24.10.2022 to 28.10.2022 in offline mode

Registration link : <https://www.aicte-india.org/atal>

Chair person : Dr.M. Suman, Professor & HoD-ECE
Coordinator : Dr.K. Srinivasa Rao, Professor & Research Group Head
Co-Coordinator : Dr. K. Girija Sravani, Associate Professor, ECE

Poster of the FDP is enclosed herewith.

REGISTRAR (I/C)

Encl: Poster

Mail & Hard copy to: Hon'ble President, KLEF

Mail to: Hon'ble Vice-Presidents, KLEF

Mail & Hard copy to: Hon'ble Pro Chancellor

Mail & Hard copy to: Hon'ble Vice Chancellor

Mail & Hard copy to: Hon'ble Pro Vice Chancellor (Administration)

Mail to: Advisor – NAAC & Hyderabad Operations - Prof. K.Koteswara Rao

Mail to: All Advisors / All Deans / All Principals / All Directors

Mail to: Controller of Examinations-Dr.A.S.C.S.Sastry

Mail to: Principal-Engg.College /HoD-Business School

Mail to: Vice-Principal-Coll. of Science & Humanities & Coordinator-FED.Dr.MSG Prasad

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HoDs..MBA / BBA / COM / HM / CSS / CA&MS / Law / Architecture / Pharmacy / CSA / Arts

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Mail to: All Dy. HoDs / All Alt. HODs

Mail to: KL H HoDs..CSE / AI&DS / ECE / Coordinator-FED

Mail to: All faculty

Mail to: All students

Mail to: All research scholars

Thanks & Regards



Dr. A. Jagadeesh
REGISTRAR (I/C)

KONERU LAKSHMAIAH EDUCATION FOUNDATION

(Category -1, Deemed to be University estd. u/s. 3 of the UGC Act, 1956)

Accredited by NAAC as 'A++' Grade University ♦ Approved by AICTE ♦ ISO 9001-2015 Certified

Campus: Green Fields, Vaddeswaram - 522 302, Guntur District, Andhra Pradesh, INDIA.

Phone No. 08645 - 350200, www.klef.ac.in; www.klef.edu.in; www.kluniversity.in

AICTE-ATL SPONSORED



TWO WEEKS FACULTY DEVELOPMENT PROGRAM ON **RECENT TRENDS IN VLSI CHIP/ DEVICES FOR SENSOR APPLICATIONS**

ORGANIZED BY
MICROELECTRONICS RESEARCH GROUP (MERG)
DEPARTMENT OF ECE
KL (Deemed to be University)
Green Fields, Vaddeswaram, Guntur(Dist),
Andhra Pradesh, INDIA-522502. www.kluniversity.in

ABOUT THE INSTITUTE

Koneru Lakshmaiah Education Foundation (KLEF) is the metamorphosis of Koneru Lakshmaiah College of Engineering (KLCE) established in 1980. It was recognized as Deemed to be University in 2009. KLEF achieved highest grade A++ awarded by NAAC, MHRD-NIRF awarded 35th rank for the university during the year 2021. ATAL Ranking of Institutions on Innovation Achievements (ARIIA) awarded KLEF rank between 6-25 during this year. KLEF bagged second prize in AICTE National Level Clean & Smart Campus for the year 2020. KLEF offers various academic programs for about 17,000 students. This University has more than 296 academic labs, 25 research labs, 6 Industry Collaborative Labs and 6 Centres of Excellencies. KLEF offers 61 programs providing several options to acquire degrees in UG, PG & Ph.D in the disciplines of Engineering, Sciences, Arts & Management. KLEF faculty are encouraged to take up research proposals from Government as well as from various funding agencies. Till now KLEF bagged funded projects worth Rs. 125 Lakhs from NGOs and Rs. 456.59 Lakhs from several Government agencies. More than 50 startups initiated which are fully functional. KLU places special emphasis on research. DSIR of Govt. of India recognized KLU as a Scientific and Industrial Research Centre. KLU has the credit of housing world class Excellency centres to boost research in emerging areas like VLSI, Nanotechnology, Robotics, Nuclear fusion, Reactor design, Automobile, Aero Space Structures etc. In order to extend R&D and consultancy activities within the university 43 faculty research groups are functioning effectively.

ABOUT THE DEPARTMENT

Department of Electronics & Communication Engineering was established in the year 1980, has grown now to be a Department with 110 Faculty members and over 2000 Under Graduate and 200 Post Graduate students and about 200 research scholars. As the largest academic Department of University, Faculty of ECE are involved in an exceptional range of Educational, Intellectual and Research activities. We have grown over the years in many directions and currently recognized as a "Premier Teaching and Research Department" of the KL University and also we recognized by DST under FIST program in the year 2012. Being a FIST-DST sponsored Department, recently we purchased the 18 GHz Network Analyser, 20 GHz Spectrum Analyser and HFSS Suite etc., In addition, the department is well equipped with various laboratories catering the UG and PG Programs and other research centres in VLSI, Communication Systems, Atmospheric Sciences and MEMS

CONTENTS TO BE COVERED

This Faculty Development Program (FDP) will provide an opportunity to learn recent research and development in the area of VLSI devices/integrated Circuits from eminent experts from IITs/NITs. The participants will have an exposure to the state-of-the-art in semiconductor device to circuit modelling, integrated circuits for Analog and Memory and Bio Sensor applications. This FDP will provide discussion/presentation on future research directions in the field of VLSI chips and applications.

The following topics will be covered:

- Emerging Semiconductor Device Technologies,
- Future Roadmap of Electronics Industry
- High Speed Memory Design,
- In Memory Boolean Computation for AI ML Applications
- Role of Semiconductor Device Modeling in for future generation electronics
- Challenges in Analog IC Design in nanoscale CMOS/FinFET technologies
- Non classical CMOS devices such as Junction-less FET
- Charge-Plasma FET and State of the Art Advanced Semiconductor Devices.
- TFET Devices for Bio-Sensor Applications
- TCAD Tools for Device Simulation

Targeted Participants

This program is open to all faculty members, P.G students, research scholars, scientists / engineers working in educational institutes / industries / R&D Organizations.

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Sri K L Havish
Vice-President, KLEF

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Principal, KL CoE

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HoD Research, KL

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Professor & HoD
Department, of ECE
KL

Coordinator
Dr.K.Srinivasa Rao
Professor,
Microelectronics & VLSI Research Group,
Department of ECE KL

Co-Coordinator
Dr.K.Girija Sravani
Assoc.Prof.,
Department of ECE, KL

Contact details
Dr.K.Srinivasa Rao
Professor,Department of ECE, KL
7095666644
drksrao@kluniversity.in



REPORT

Recent Trends in VLSI Chip/ Devices for Sensor Applications

Date: 02-11-2022, Koneru Lakshmaiah Education Foundation (Deemed to be University), Guntur, Andhra Pradesh

Recent Trends in VLSI Chip/Devices for Sensor Applications

VLSI chip/ Devices for sensor applications, AICTE sponsored FDP was conducted from 26th September to 1st October 2022 in Online mode, 26th October to 28th October 2022 in offline in which around 50 participants from different parts of the country participated.

The speakers for the Two week FDP “Recent Advancements in VLSI Chip/ Devices for Sensor Applications” were:

ON-Line Speakers

Dr. Koushik Guha Assoc. Prof, NIT Silchar



Education

- **Ph.D.:** National Institute of Technology Silchar, Assam, India, 2016
- **M.Tech.:** Burdwan University, West Bengal, India, 2007
- **B.Tech.:** West Bengal University of Technology, Kolkata, India, 2005

Experience

- **06 July 2022 to present: Associate Professor**, National Institute of Technology Silchar
- **01 Jun 2018 to 06 July 2022: Assistant Professor Grade-I**, National Institute of Technology Silchar.
- **Jun 2010 to 31 May 2018: Assistant Professor Grade-II**, National Institute of Technology Silchar.
- **27 Aug 2007 to 14 Jun 2010: Lecturer**, Haldia Institute of Technology, Department of Electronics and Communication Engineering, W. B, India.
- **2005-2007 -Software Engineer**, IBM India Pvt Ltd




Education

Postdoc-2011 VLSI Design (University of Rome, Italy)
Ph.D-2010 Microelectronics and VLSI Design (IIT Roorkee)
M.Tech-2006 Microelectronics (Panjab University Chandigarh)
B.Tech-2004 Electronics Engineering (Punjab Technical University)

Experience

2019 – Present: **Associate Professor.ECE,NIT ,Chandigarh**
2012 – 2019: **Assistant Professor ECE**
Dr B R Ambedkar National Institute of Technology, Jalandhar
2011 – 2012: **Assistant Professor**
ABV-Indian Institute of Information Technology and Management, Gwalior


ATAL FDP Program on Recent Trends in VLSI Chip/Devices for Sensor Applications

	<ul style="list-style-type: none"> • Ph.D. Central University, 2009 • M.Tech BITS Pilani, 2006
	Experience <ul style="list-style-type: none"> • April 2015 - present: Professor, EceDept KLEF • February 2010 - March 2015 :Professor & HOD, EIE <u>Lakireddy Bali Reddy College of Engineering.</u> • July 2006 - June 2009: <u>Assistant Professor Assam University.</u>

Dr Balwinder Raj, Assoc. Prof NITTTR Chandighard.

Dr.K.Srinivas Rao, KL University

Dr.Suman lata Tripathi.professor lovely professional university.punjab.


	Education <ul style="list-style-type: none"> • Ph.D. in the area of microelectronics and VLSI from MNNIT, Allahabad. 2015 • M.Tech UP Technical University, 2010
	Experience <ul style="list-style-type: none"> • Jan 2019 - present: Professor lovely professional university.punjab • Jan 2017 - Jan 2019 : Assistant Professor , lovely professional university.punjab

Dr. Y.Naresh, Malla Reddy University.

ATAL FDP Program on Recent Trends in VLSI Chip/Devices for Sensor Applications

	<p>Education</p> <p>Experience Jan 2017 - present: : Assistant Professor , Malla Reddy University</p>
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Dr.Keethi Assoc Professor, JNTUH

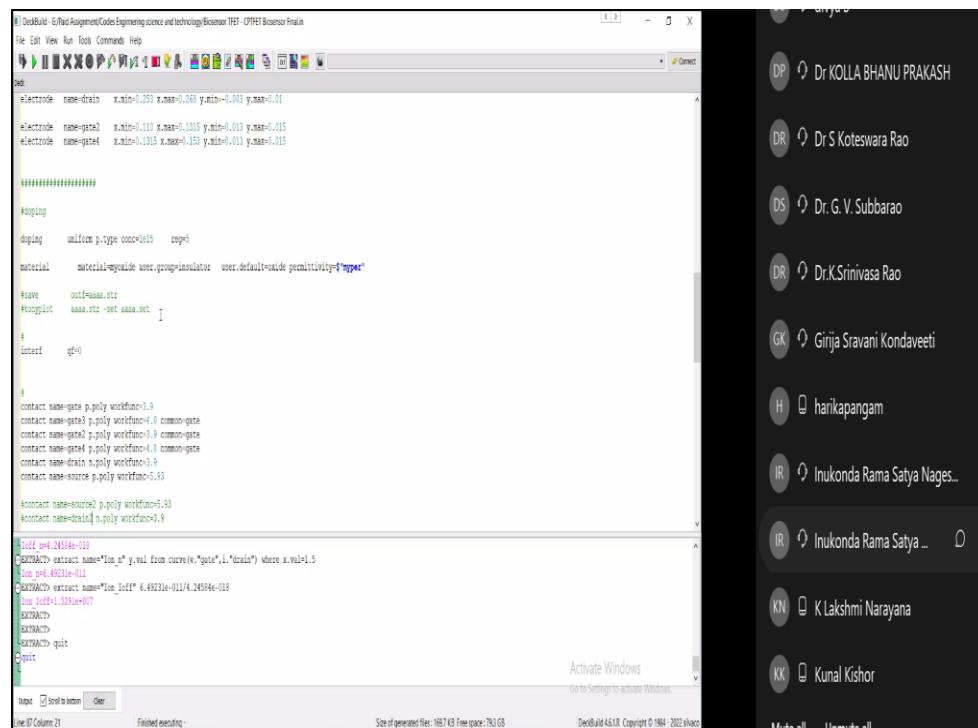
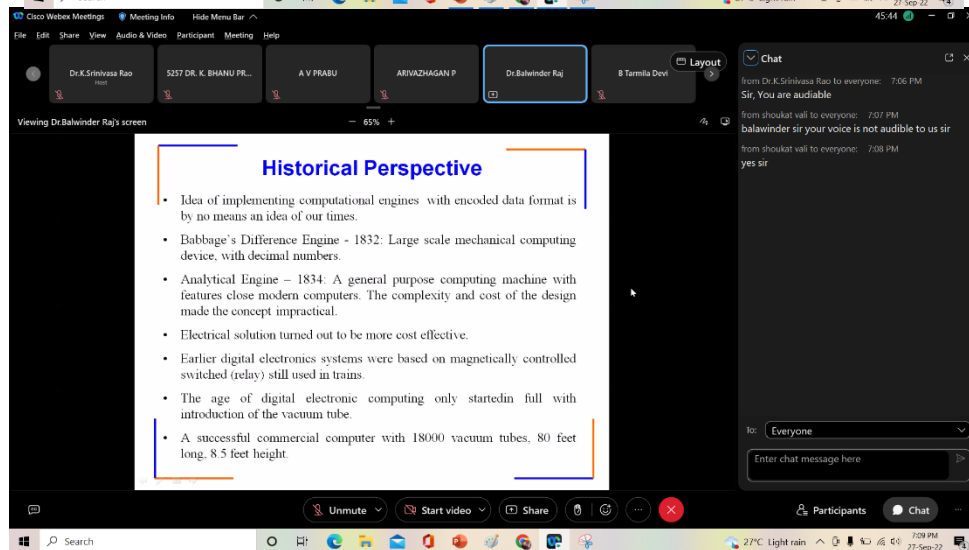
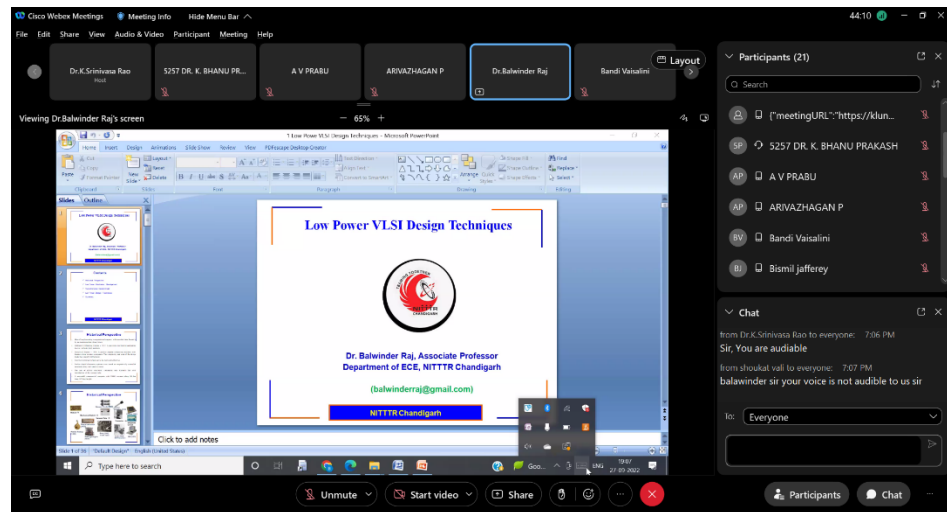
	<p>EDUCATION</p> <p>B.Tech: - Electronics and Communication Engineering, Malla Reddy College of Engineering For Women-Suraram, Hyderabad 2014.</p> <p>M.Tech: - VLSI System Design, BVRaju Institute of Technology, Narsapur 2016</p> <p>EXPERIENCE</p> <p>2017-present:Dr.Keethi Assoc Professor, JNTUH</p>
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Online Schedule:

DATE	SPEKER	TITLE
26-09.2022	Dr. Koushik Guha Assoc. Prof, NIT Silchar	Recent Trends in CMOS, Emerging Devices and Technology in VLSI Design for Biomedical Applications
27-09.2022	Dr.Balawindar Rai , NITTR Chandigarh	TFET Devices for Bio-Sensor Applications
28-09.2022	Dr.K.Srinivasa Rao , KL University	Charge-Plasma FET and State of the Art Advanced Semiconductor Devices
29-09.2022	Dr.Suman Latha Tripathy , LPU	Hands-On Session TCAD Tools for Device Simulation
30-09.2022	Dr. Y.Naresh , Malla Reddy University Malla Reddy University	Non classical CMOS devices such as Junction-less FET
1-10.2022	Dr.Keethi Assoc Professor, JNTUH	TCAD Tool for TFET Device Simulation-Hands on Training

Somescreenshotsoftheareasbelow.

ATAL FDP Program on Recent Trends in VLSI Chip/Devices for Sensor Applications



ATAL FDP Program on Recent Trends in VLSI Chip/Devices for Sensor Applications

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Suman Lata Tripathi Dr.K.Srinivasa Rao ARIVAZHAGAN P B Tarmila Devi Bandi Vaisalini Bismil jafferey Layout

Viewing Suman Lata Tripathi's screen 91% +

Challenges in Analog IC Design in nanoscale CMOS/FinFET technologies, 26th September 2022 - PowerPoint Suman Lata Tripathi

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AT&T AICTE National Workshop
on
Recent Trends in VLSI Chip/ Devices for Sensor Applications
from 26th September to 1st October-2022
Challenges in Analog IC Design in nanoscale
CMOS/FinFET technologies
29th September-2022
Organized by
KL University, Guntur

Dr Suman Lata Tripathi
Professor, VLSI Design
School of Electronics and Electrical Engineering
Lovely Professional University, Punjab, India-144411
Post-Doc Researcher, Department Computer Science
Nottingham Trent University UK

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29°C Haze 19:10 29-09-2022

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Participants (12)

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SV shoukat vali Host, me

ST Suman Lata Tripathi

AP ARIVAZHAGAN P

BD B Tarmila Devi

BV Bandi Vaisalini

BJ Bismil jafferey

B boobalan

DC Dr Joshitha C

DR Dr.K.Srinivasa Rao

D drksrao

GK Girija Sravani Kondaveeti

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Participants Chat

29°C Haze 7:10 PM 29-Sep-22

For Non Planar Junction

(1) For tunneling through non-planar junctions, it is preferable to construct a complicated polygonal region to use the BBT.NONLOCAL method.

(2) You can achieve this by using several joined QTREGION's. The simple rule that must be followed to join the quadrilaterals is to ensure that point (X2, Y2) of the first quadrilateral matches with (X1, Y1) of the second quadrilateral, and that point (X3, Y3) on the first matches point (X4, Y4) on the next.. In this way, you can build up a tunneling mesh to cover quite complicated p-n junction shapes.

(3) You must set up the number of mesh points you require in the tunneling direction and the simplest way to do this is to use the PTS.TUNNEL parameter. The value of PTS.TUNNEL applies to all slices in a region of one or more joined quadrilaterals.

p-n junction (X3,Y3)

(X2,Y2)

The first QTREGION must have all 4 corner points described.

Fig. Example of a polygonal region made by joining 4 quadrilaterals to cover quite complicated p-n junction shapes

Activate Windows
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DR Dr S Koteswara Rao

DS Dr. G. V. Subbarao

DR Dr.K.Srinivasa Rao

GK Girija Sravani Kondaveeti

H harikapangam

IR Inukonda Rama Satya Nages...

IR Inukonda Rama Satya ...

KN K Lakshmi Narayana

KK Kunal Kishor

LP Lakshman Pappula

Mute all Unmute all

ATAL FDP Program on Recent Trends in VLSI Chip/Devices for Sensor Applications

OFF-LINE SPEAKERS:

Prof. Ramesh Vaddi, Associate Professor & HoD, SRM University, Andhra Pradesh



Education

PHD:2011 IIT Roorkee

M.Tech: 2004**MANIT Bhopal.**

BTech: 2002MVGR College of Engg, Vizianagaram,JNTU Hyderabad

Experience

- 06/2019- Till Date, Associate Professor, Electronics and Communication Engineering | Department, School of Engineering and Applied Sciences, SRM University, Amaravati, Guntur, AP, India
- 06/2018- 05/2019, Senior Research Fellow, School of Computing, National University of Singapore, Singapore.
- 6/2015-05/2018, Assistant Professor, Electronics and Communication Engineering, DSPM International Institute of Information Technology-Naya Rapur Chhattisgarh, India.
- 1/2014-06/2015, Assistant Professor, Electrical Engineering Department, School of Engineering, Shiv Nadar University, Greater Noida, UP, India.
- 2/2013- 08/2013, Postdoc Scholar, Department of Computer Science and Engineering, The Pennsylvania State University, University Park, PA, USA.
- 6/2012-1/2013, Professor, Electronics and Communication Engineering Department, Padmasri Dr. B. V. Raju Institute of Technology (BVRIT), Hyderabad, India.
- 2/2011-4/2012, Postdoctoral Research Fellow, VIRTUS (IC Design Centre of Excellence), Circuits and Systems Division, School of Electrical and Electronic Engineering, Nanyang Technological University, 50 Nanyang Avenue, Singapore.
- 8/2005-12/2007, Assistant Professor, Electronics and Communication Engineering Department, College of Engg, GITAM University, Vizag, India.
- 7/2004-8/2005, Lecturer (Ad-hoc), Electronics and Communication Engineering Department, Maulana Azad National Institute of Technology, Bhopal, India

ATAL FDP Program on Recent Trends in VLSI Chip/Devices for Sensor Applications

Dr.Ch.Pulla Rao,Associate Professor , JNTU K



Education

PHD:JntuK

Mtech:NIT Warangal.

BTech:AMIETE

Experience

May 2015 – Present:Head of the Department ECEHead of the Department ECE

Devineni Venkata Ramana & Dr. Hima Sekhar MIC College of Technology.

May 2010 - May 2015:Assistant ProfessorAssistant Professor
Lakireddy Bali Reddy College of Engineering

Dr.Deepak Kumar Panda,Associate Professor,,School of Electronics and Engineering,VIT-AP.



Education

PHD:2018 NIT,Silchar.

M.Tech: 2014 IIT Kharakpur.

B.Tech: (NIST), Berhampur

Experience

Jul 2010 - Jul 2014:Assistant ProfessorAssistant Professor
National Institute of Science and Technology (NIST), Berhampur · Full-time.

May 2018 – Present:Associate Professor
VIT-AP · Full-time

ATAL FDP Program on Recent Trends in VLSI Chip/Devices for Sensor Applications

Dr.A.Narendra Babu,LBRCE, JNTU Kakinada



EDUCATION

PhD: SV University,2008.

PG : SV University,2001.

EXPERIENCE

31-08- 09-present:Professor, LBRCE.

01-07- 2002- 31-08- 2007: Teaching Assistant, SV University.

Dr. Neerai Kumar Misra,Associate Professor (SENSE),Vellore Institute of Technology (VIT)-AP



EDUCATION

PHD: Dr. A.P.J. Abdul Kalam Technical University: Lucknow, Uttar Pradesh, IN ,2017.

M.Tech:Amity ,Lucknow.

BTECH: Integral University: Lucknow, Uttar Pradesh, IN

EXPERIENCE

Jun 2022 – Present: Associate ProfessorVIT-AP ·

Jan 2018 - May 2022:Associate Professor

Bharat Institute of Engineering & Technology

Jul 2017 - Jan 2018 :Associate Professor

Bharat Institute of Engineering & Technology

ATAL FDP Program on Recent Trends in VLSI Chip/Devices for Sensor Applications

Pranitha, Assoc Professor, JNTU Kakinada



EDUCATION

Pursuing Ph.D in K.L. University, Guntur, Andhra Pradesh

M.Tech - CSE from JNTUK, Kakinada in 2014.

MSc - CSE from S.V. University, Tirupathi in 2002.

EXPERIENCE

2017 – Present- **Assistant Professor**

CSE

Lakireddy Bali Reddy College of Engineering (Autonomous), Krishna

Dr. G. Amarnath, Associate Professor & Associate Dean (R&D) ECE. Marri Laxman Reddy Institute of Technology and Management, Hyderabad



EDUCATION

Ph.D. degree in Microelectronics and VLSI(ECE) in Feb-2019 from NIT-Silchar, India. M.Tech. degree in VLSI System Design in

2009 and B.Tech. degree in ECE in

2007, from Jawaharlal Nehru Technological University, Hyderabad

EXPERIENCE

2019-present: **Associate Professor & Associate Dean (R&D)**

Department of Electronics & Communication Engineering

Marri Laxman Reddy Institute of Technology and Management,
Hyderabad

ATAL FDP Program on Recent Trends in VLSI Chip/Devices for Sensor Applications

Dr.Y Naresh, ML University



EDUCATION

EXPERIENCE

Dr.Keethi Assoc Professor, JNTUH



EDUCATION

B.Tech: - Electronics and Communication Engineering, Malla Reddy College of Engineering For Women-Suraram, Hyderabad 2014.

M.Tech: - VLSI System Design, BVRaju Institute of Technology, Narsapur 2016

EXPERIENCE

2017-present:Dr.Keethi Assoc Professor, JNTUH

ATAL FDP Program on Recent Trends in VLSI Chip/Devices for Sensor Applications

OFF line Schedule:

DATE	SESSION	SPEKER	TITLE
24-10.2022	FN	Prof. Ramesh Vaddi Associate Professor & HoD, SRM University, AP.	Nano Scale Devices and Circuits For Energy Efficient On-chip VLSI Accelerators for ML and Hardware Security Primitives
24-09.2022	AN	Dr.Ch.Pulla Rao, Associate Professor , JNTU K	Future roadmap Electronics Industry and Recent developments of semiconductor nanoscale devices
25-10.2022	FN	Dr.Deepak Kumar Panda Associate Professor, School of Electronics and Engineering, VIT-AP	TFET based Biosensor for Label-Free Detection of Biomolecules
25-10.2022	AN	Dr.A.Narendra Babu LBRCE, JNTU Kakinada	Charge-Plasma FET and State of the Art Advanced Semiconductor Devices for VLSI design automation
26-10.2022	FN	Dr. Neeraj Kumar Misra Associate Professor School of Electronics Engineering (SENSE), Vellore Institute of Technology (VIT)-AP	Computing and Architecture Beyond CMOS for the Future Electronics Roadmap
26-10.2022	AN	Dr.Pranitha Assoc Professor, JNTU Kakinada	Semiconductor devices and Engineering solutions towards Industry Needs
27-10.2022	FN	Dr. G. Amarnath, Associate Professor & Associate Dean (R&D) Department of Electronics & Communication Engineering Marri Laxman Reddy Institute of Technology and Management, Hyderabad	GaN HEMTs and its Modeling for RF and Power Electronic Applications
27-10.2022		Dr.Y Naresh, ML University	"TCAD-Circuit simulation by Synopsys"
28-10.2022		Dr.Keethi, JNTUH	TCAD Tool for TFET Device Simulation-Hands on Training

ATAL FDP Program on Recent Trends in VLSI Chip/Devices for Sensor Applications

Second one Week OFFLINE Course Sessions ()

Day-1 (26/10/2022)

Session-1: Morning Session: We have called **Dr.Ramesh Vaddi** from **SRM University** for first day morning session and he gave a talk "Nanoscale Devices and Circuits for Energy Efficient on Chip VLSI Accelerators for ML and Hardware Security Primitives".

We have Lunch Session, arranged at SAC, R&D Building Ground Floor for 60+ Members from Department of ECE, HoD, Deans, RPACs, Technical Members etc.

Industrial Visit Session.

Session-2: Afternoon session we have **Dr.Ch.Pullu Rao**, given talk on "**Future roadmap Electronics Industry and Recent developments of semiconductor nanoscale devices**".

Day-2 (27/10/2022)

Session-3: **Dr.Deepak Kumar Panda** from **VIT University** has given a talk on "**TFET based Biosensors for label free detection of biomolecules**". He has given clear understanding about TFET devices and its issues and possible solutions.

We have Lunch Session, arranged at SAC, R&D Building Ground Floor for 60+ Members from Department of ECE, HoD, Deans, RPACs, Technical Members etc.

Industrial Visit Session.

Session-4: **Dr.A.Narendra Babu**, LBRCE, JNTU Kakinada has given a talk on "**Charge-Plasma FET and State of the Art Advanced Semiconductor Devices for VLSI design automation**".

Day-3 (28/10/2022)

Session-5: **Dr.Neeraj Kumar Mishra** from **VIT University** given a talk on "**Computing and Architecture beyond CMOS for the future Electronics roadmap**". She has focus on TFET devices, particularly Charge Plasma FET for Bio-Sensing applications.

We have Lunch Session, arranged at SAC, R&D Building Ground Floor for 60+ Members from Department of ECE, HoD, Deans, RPACs, Technical Members etc.

Industrial Visit Session.

Session-6: **Dr.Pranitha**, JNTU Kakinada has given a talk and hands on session "**Semiconductor devices and Engineering solutions towards Industry Needs**".

Day-4 (29/10/2022)

ATAL FDP Program on Recent Trends in VLSI Chip/Devices for Sensor Applications

Session-7: **Dr.G Amarnath** from **MLRIT** has given a talk on "**GaN HEMTs and its modeling for RF and Power Electronic Applications**". He has talk about present state of all kind of VLSI Chip Devices and its applications.

We have Lunch Session, arranged at SAC, R&D Building Ground Floor for 60+ Members from Department of ECE, HoD, Deans, RPACs, Technical Members etc.

Session-8: **Dr.Y Naresh**, **ML University** has given hands on session "TCAD-Circuit simulation by Synopsys".

Session-9: Last Session is talk given by **Dr.Keethi**, **JNTUH** on "TCAD Tool for TFET Device Simulation-Hands on Training".

The total number of participants for this workshop is 50 members; they have attended from around the state, few members from out of state too. The organizing committee has done excellent job, without any discrepancy and disturbance in any aspects.. Finally, as Convener **Dr.K.Srinivasa Rao** and Co-Convenors says vote of thanks to resources, & participants for making the workshop a grand success.

SOME PhotosOf The Sessions:



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Participants:

Name	application_number	Institute Name	Designation
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Dr. Lakshman Pappula	1649329521	KLEF (Deemed to be University)	Associate Professor
Dr. Suman Lata Tripathi	1649329521	Lovely Professional University	Professor
Dr. Fazal Noorbasha	1649329521	K L University	Associate Professor
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Mr. Pamarthi Naga Basaveswara Swamy	1649329521	NRI INSTITUTE OF TECHNOLOGY	Assistant Professor



This is to certify that

DR. ADITYA JAPA

Has participated in the

Two-Weeks Faculty Development Program on

“Recent trends in VLSI Chip devices/Circuits for Sensor Applications”

During 26.09.2022 to 01.10.2022 and 24.10.2022 to 28.10.2022


Principal
ASC