Conduction of a Five-day Faculty Development Program (FDP) on "Shrinking the Future: Cutting-Edge Trends in VLSI Design" organized by Microelectronics Research Group (MERG), ECE from 29-06-2024 to 04-07-2024 - Reg.

Registrar <registrar@kluniversity.in>

Wed 2024-06-26 12:42 PM

To:Prof. Chandra Prakash <vchandrap@kluniversity.in>;Dr V Srikanth <vsrikanth@kluniversity.in>;Dean - Placements & Internships (International)-K L University <nbvprasaad@kluniversity.in>;K R S Prasad <krsprasad_fed@kluniversity.in>;N Venkat Ram <venkatram@kluniversity.in>;Slavanya <slavanya_css@kluniversity.in>;Shanmukh <shanmukh_fed@kluniversity.in>; Director-CRT <mvn@kluniversity.in>;prasanth <prasanthyalla@kluniversity.in>;Suman Maloji <suman.maloji@kluniversity.in>; Dr.I.Govardhani <govardhanee_ec@kluniversity.in>;Dr. G. Dinesh Kumar <dinesh@kluniversity.in>;Vemuri Praveen Kumar <vemuripraveen@kluniversity.in>;Sri Kavya K Ch <kavya@kluniversity.in>;loveswra rao Burthi <loveswararao@kluniversity.in>; Ram Prasad <avsrp_me@kluniversity.in>;Radhika Rani Chintala <radhikarani_cse@kluniversity.in>;ravi kumar <ravikumar@kluniversity.in>;Dr. Shaik Razia <skrazia@kluniversity.in>;PavanKumar <pavankumar_ist@kluniversity.in>
Cc:PRESIDENT <president@kluniversity.in>;H . <h@klh.edu.in>;Raja Harin koneru <krh@kluniversity.in>;PRO-CHANCELLOR <prochancellor@kluniversity.in>;Vice Chancellor - KLU <vc@kluniversity.in>;Dr.G.P.S. Varma, Vice- Chancellor <gpsvarma@kluniversity.in>;Pro VC <provc@kluniversity.in>;N Venkat Ram <venkatram@kluniversity.in>;Pro-VC-Academics <provc-academics@kluniversity.in>;Dr Jagadeesh Anne <drjagadeesh@kluniversity.in>

1 attachments (520 KB)

SHRINKING THE FUTURE cutting edge trends in VLSI Design.pdf;

Ref: KLEF/RO/ASC/ECE/FDP/2023-24 26st June 2024

Orders of the Hon'ble Vice-Chancellor dt. 26-06-2024

CIRCULAR

Sub: Conduction of a Five-day Faculty Development Program (FDP) on "Shrinking the Future: Cutting-Edge Trends in VLSI Design" organized by Microelectronics Research Group (MERG), Department of Electronics and Communication Engineering, KLEF, Vaddeswaram, in association with Academic Staff College, from 29 June 2024 to 04 July 2024 (Excluding 30.06.2024, Sunday) - Communication – Reg.

Ref: Letter received from Dr. Debajit Deb, Assistant Professor & FDP Coordinator, ECE and forwarded by Dr.M. Suman HoD-ECE & Principal, Academic Staff College.

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This is to inform that a five-day Faculty Development Program (FDP) on "Shrinking the Future: Cutting-Edge Trends in VLSI Design" organized by Microelectronics Research Group (MERG), Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation, Vaddeswaram, in association with Academic Staff College, from 29 June 2024 to 04 July 2024 (Excluding 30.06.2024, Sunday).

This FDP aims to equip participants with in-depth knowledge and understanding of the latest advancements and emerging trends in the field of VLSI design. The program will cover a wide range of topics, including:

- Beyond Moore's Law: Exploring new materials and technologies for transistor scaling.
- The Rise of AI Hardware: Understanding the role of VLSI design in on-chip intelligence.
- Low-Power VLSI Design: Techniques for optimizing power consumption in integrated circuits.

- VLSI Design for Security: Hardware-based solutions for mitigating security threats.
- Emerging Applications of VLSI Design: Exploring the use of VLSI design in various fields such as IoT, machine learning, and biomedical engineering.

e-FDP Details:

Date and Time: 29 June 2024 to 04 July 2024.
FDP Duration: 9:30 AM to 1:30 PM
Registration Fee: Free (For Internal Candidates)
: Rs. 500/- (For External Candidates)

Who can Attend: All Engineering faculty

e-FDP Registration Link:

https://docs.google.com/forms/d/e/1FAIpQLSdQKvKHVV0L5zyf3Rv-UO7L5RivKChdBekFZrKuf1HIVD792A/viewform

Organizing Committee: Microelectronics Research Group, Department of ECE, KLEF
Coordinator: Dr. Debajit Deb, Asst. Professor, Dept. of ECE, KLEF.

Brochure of the e-FDP with program schedule is enclosed herewith.

REGISTRAR

Encl: as above

Mail & Hard copy to: Hon'ble President, KLEF
Mail to: Hon'ble Vice-Presidents, KLEF
Mail & Hard copy to: Hon'ble Pro Chancellor
Mail & Hard copy to: Hon'ble Vice-Chancellor
Mail & Hard copy to: Pro Vice-Chancellors
Mail to: Chief Coordinating Officer-Dr.A. Jagadeesh
Mail to: Special Officer -Dr.A. Vani
Mail to: All Advisors / All Deans / All Principals / All Vice-Principals / All Sr.Directors / All Directors / All Additional Deans /
All Associate Deans / Deputy Deans / PR Head
Mail to: Controller of Examinations-Dr.A.S.C.S.Sastry
Mail to: Joint Registrar / Deputy Registrar / Sr.Manager (Alumni Relations) & AR-Sri A.Krishna Rao / AR-Dr.MVAL Narasimha Rao
Mail to: Advisor – NAAC & Hyderabad Operations - Prof. K.Koteswara Rao
Mail to: Principal-CoE..Dr.T.K. Rama Krishna Rao / Coordinator-FED..Dr.MSG Prasad / Dy.Coordinator-FED..Dr.J.Somlal
Vice-Principals
Mail to: All HoDs
Mail to: All Dy. HoDs / All Alt. HoDs
Mail to: KL H - Principal Off Campus Centre, Aziz Nagar Campus / KL H - Principal Off Campus Centre, Bowrampet

Vice-Principal / Director / Deputy Director

Mail to: KL H HoDs.. AI&DS / CSE / ECE / BES / FED Coordinator / Business School

Mail to: KL H Associate Deans..P&D / R&D / Academics / IQAC / F&SA / Skill Development / Student Progression & Training /

Student Affairs / Student Welfare / Examinations

Mail to: Librarian

Mail to: Webmaster-Mr.LV

Mail to: Chief Technical Officer (CTO)-Mr.A.Satya Kalyan

Mr. Raja Sekhar, Emp. No. 2482, Jr. Network Administrator (E-mail: rajasekhar_syte@kluniversity.in)

Mail to: Professor In-charge, EduTech, Animation-Dr. M. Siva Kumar,Assoc. Professor,ECE

Mail to: Principal-Academic Staff College

HoD-ECE & Additional HoD-ECE

Dr. Debajit Deb, Assistant Professor & FDP Coordinator, ECE

All Engineering Faculty

Thanks & Regards

Dr. K. Subba Rao
REGISTRAR
KONERU LAKSHMAIAH EDUCATION FOUNDATION
(Category -1, Deemed to be University estd. u/s. 3 of the UGC Act, 1956)
Accredited by **NAAC** as '**A++**' Grade University ❖Approved by AICTE ❖ ISO 21001:2018 Certified
Campus: Green Fields, Vaddeswaram - 522 302, Guntur District, Andhra Pradesh, INDIA.
Phone No. **08645 - 350200**; **www.klef.ac.in; www.klef.edu.in; www.kluniversity.in**

Registration Form

1. Name.....
2. Designation .....
3. Name and Address of the Organization
   .....
   .....
4.Phone No: .....
5. E-Mail: .....

6.Address for Correspondence :
.....
.....

Account Details for Payment:
Account No. : 62162871052
Account Name : Koneru Lakshmaiah Education Foundation
IFSC Code: SBIN0021361
Registration Fee: Rs. 500 (Outside KLEF)

Link of Registration:
https://forms.gle/AjPDvMvDNruxvere6

Contact Detail of the Coordinator

Dr. Debajit Deb
Assistant Professor,
Department of ECE
Koneru Lakshmaiah Education Foundation
(Deemed to be University)
Green Fields, Vaddeswaram, Guntur, AP, INDIA
Mobile:7005786066/9485158291
E-mail: debajitdeb@kluniversity.in

KL UNIVERSITY (DEEMED TO BE)

KL Academic Staff College

SHRINKING THE FUTURE

Cutting-Edge Trends in VLSI Design

Faculty Development Program

June 29th – 04thJuly,2024

Organized by
Microelectronics Research Group (MERG)
Department of ECE
In association with
Academic Staff College

Chairperson
Dr. M.Suman
HOD, Department of ECE
Co-Chairperson
Dr. K. Srinivasa Rao,
Addl. HOD, ECE, KLEF

Koneru Lakshmaiah Education Foundation
(Deemed to be University)
Green Fields, Vaddeswaram, Guntur(Dist),
Andhra Pradesh, INDIA-522302.
www.kluniversity.in

About the Organisation

The Koneru Lakshmaiah Charities was established as a trust in the year 1980 with its official address at Museum road, Governorpet, Vijayawada, Andhra Pradesh 520 002 and started KL College of Engineering in the Academic year 1980-81. KLEF Deemed to be University was established in 1980-81, as KL College of Engineering, which was upgraded to KL College of Engineering Autonomous in 2006 by UGC, and was declared as a Deemed to be University in 2009 by UGC, MHRD Govt.of India. In 2012 as a Deemed to be University the institution was accredited by NAAC with A Grade and later in 2018, was re-accredited by NAAC with A++ grade. In 2019 UGC, MHRD declared this institution as Category I Institution.

Vision

To be a globally renowned university.

Mission

To impart quality higher education and to undertake research and extension with emphasis on application and innovation that cater to the emerging societal needs through all-round development of the students of all sections enabling them to be globally competitive and socially responsible citizens with intrinsic values.

About ASC-KLEF

The Academic Staff College (ASC-KLEF) was established in 2009 and has since changed often to meet the demands of staff members and pertinent partners in terms of learning, training, and knowledge management. Since our founding as an interagency learning institution, we have grown to be important global partners for a vast network of stakeholders. Each year we offer over 50 programs to over 4,400 professionals. Either online, face-to-face, or a combination of both, our learning solutions deliver high-quality learning experiences that support professionals along their learning journeys. We have a wide range of options for both on-campus and online learning, depending on the program you select.

About the Department

Department of Electronics & Communication Engineering was established in the year 1980, has grown now to be a Department with 110 Faculty members and over 2000 Under Graduate and 200 Post Graduate students and about 200 research scholars. As the largest academic Department of University, Faculty of ECE are involved in an exceptional range of Educational, Intellectual and Research activities. We have grown over the years in many directions and currently recognized as a "Premier Teaching and Research Department" of the KL University and also we recognized by DST under FIST program twice. The department is well equipped with various laboratories catering the UG and PG Programs and other research centres in VLSI, Communication Systems, Atmospheric Sciences and MEMS.

Objectives of the FDP

This FDP will provide an opportunity to learn recent research and development in the area of VLSI devices/Integrated Circuits from eminent experts from IITs/NITs. The participants will have an exposure to the state-of-the-art in semiconductor device to circuit modelling, integrated circuits for Analog and Memory and applications. This workshop will provide discussion/presentation on future research directions in the field of VLSI chips and applications.

Research at KLEF

KLEF places special emphasis on research. CSIR of Govt. of India recognized KLEF as a Scientific and Industrial Research Centre. KLEF has the credit of housing world class Excellency centres to boost research in emerging areas like VLSI, Nanotechnology, Robotics, Nuclear fusion, Reactor design, Automobile, Aero Space Structures etc. In order to extend R&D and consultancy activities within the university 43 faculty research groups are functioning effectively. Funded projects of worth more than 10 Crores are sanctioned & more than 5 Crores are in pipeline, which speaks about the strength of the outsourced research at KLEF.

Topics covered

- ✓MEMS and Nanoelectronics
- ✓Analog VLSI Design
- ✓VLSI Testing
- ✓Mixed-Signal Circuit & System
- ✓ASIC-Chip Tape-out & Testing
- ✓Semiconductor Device Modeling
- ✓FPGA Implementation of Digital Design
- ✓Advanced Functional Materials and Devices

Schedule

Date/ Session	9:40 AM-11.20 AM	11.40 AM-1:20 PM
29.06. 2024	Dr B.K Mahajan ,Purdue University,Indiana, USA	Dr Pritam Bhattacharjee, VIT Chennai, India
01.07.2024	Dr.Alak Majunder, NIT Arunachal Pradesh	Dr. Bijit Choudhury, NIT Silchar
02.07.2024	Dr.Naresh Kumar Reddy, NIT Trichy	Dr.Balwinder Raj, NIT Jalandhar
03.07. 2024	Dr. Siddhanth Roy,Global Foundries	Dr. Gopal Rawat , IIT Mandi
04.07.2024	Dr. Bikram Paul, BITS Pilani	Dr. Surya Prakash M NIT Culicut

Instructions to Participants

- This Program is open to all Faculty Members , Research Scholars , PG Students , Scientists , Engineers working in Educational Institutes/ Industries / R&D Organizations.
- Certificates will be provided after succesful completion of FDP (75% Attendance)

Report on

Five-Day Faculty Development Program on

"Shrinking the Future: Cutting Edge Trends in VLSI Design"

D: 29-06-2024 to 4-7-2024

Academic Staff College in association with Microelectronics Research Group (MERG), Department of ECE conducted a five-day Faculty Development Program on "**Shrinking the Future: Cutting Edge Trends in VLSI Design**" from June 29th – 04th July 2024 with a target of enriching faculties with basic as well as advanced contents related to VLSI. There were contributed lectures by resource persons with strong academic/industrial backgrounds over the entire tenure of FDP. Resource persons were also from eminent government institutes like NITs/IITs and VLSI industries like Texas Instruments, Global Foundries, etc. There were two sessions every day from 9:40 AM-11:20 AM (Session 1) and 11:40 AM – 1:20 PM (Session 2). Around 95 participants have registered and participated in the program including faculties, research scholars and other academicians across different parts of the country.

Program Schedule:

Date	Session 1 (9:40 AM-11.20 AM)		Session-2 (11.40 AM-1:20 PM)
29.06. 2024	Dr B.K Mahajan , Texas Instruments, Dallas, USA.	B R E A K	Dr Pritam Bhattacharjee, Vellore Institute of Technology, India.
01.07.2024	Dr.Alak Majunder, NIT Arunachal Pradesh.		Dr. Bijit Choudhury, NIT Silchar.
02.07.2024	Dr.Naresh Kumar Reddy, NIT Trichy.		Dr.Balwinder Raj, NIT Jalandhar.
03.07. 2024	Dr. Siddhanth Roy, Global Foundries.		Dr. Gopal Rawat, IIT Mandi.

04.07.2024	Dr. Bikram Paul, BITS Pilani.		Dr. Surya Prakash M, NIT, Calicut.

Resource Persons:

DR. BIKRAM K MAHAJAN
PURDUE UNIVERSITY, USA

DR. PRITAM BHATTACHARJEE
VIT CHENNAI, INDIA

DR. ALAK MAJUMDER
NIT ARUNACHAL PRADESH

DR. BIJIT CHOUDHURI
NIT SILCHAR

DR. BIKRAM PAUL
BITS PILANI

DR. BALWINDER RAJ
NITJALANDHAR

DR. SIDDHANTA ROY
GLOBAL FOUNDRIES

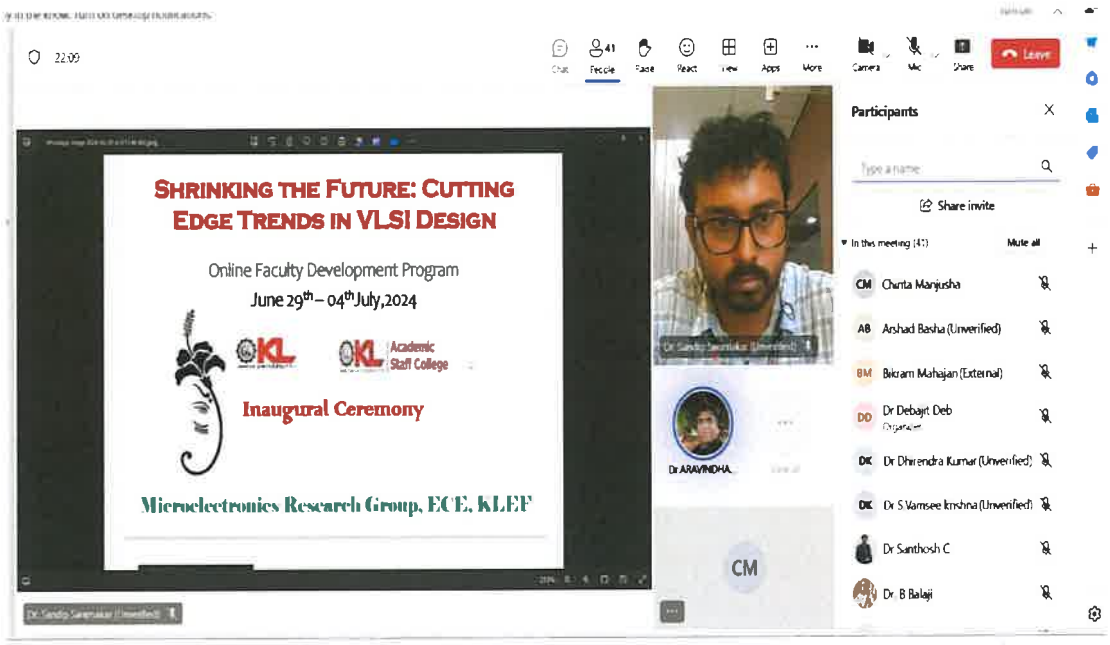
DR. GOPAL RAWAT
IIT MANDI

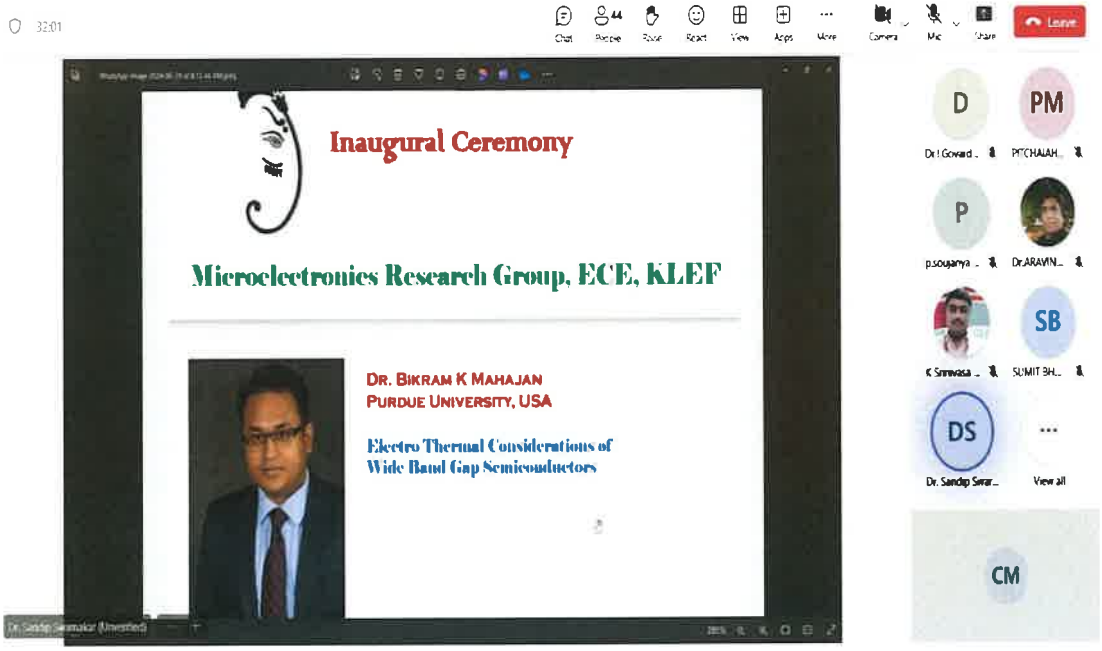
DR. B. NARESH KUMAR REDDY
NIT TIRUCHIRAPALLI

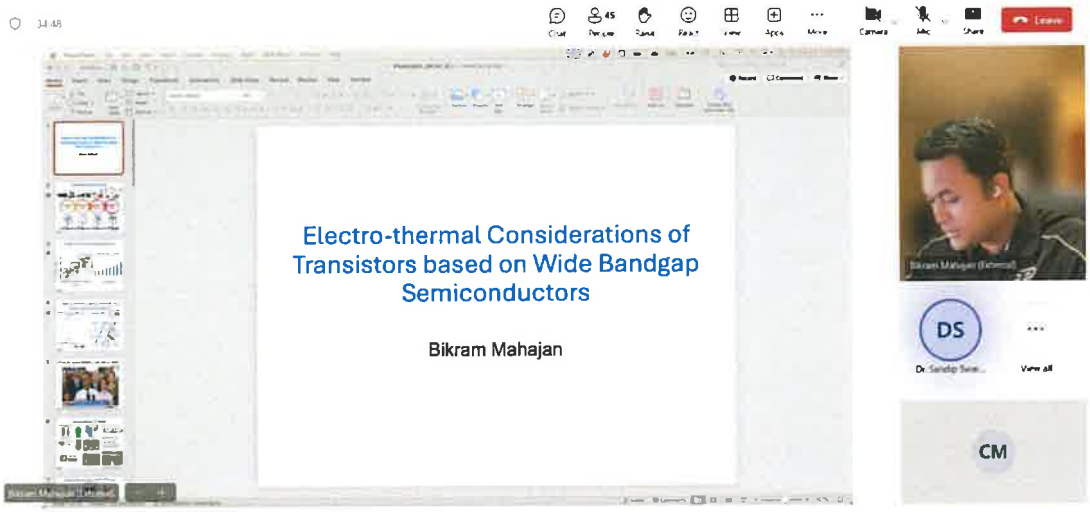
DR. M. SURYA PRAKASH
NIT CALICUT

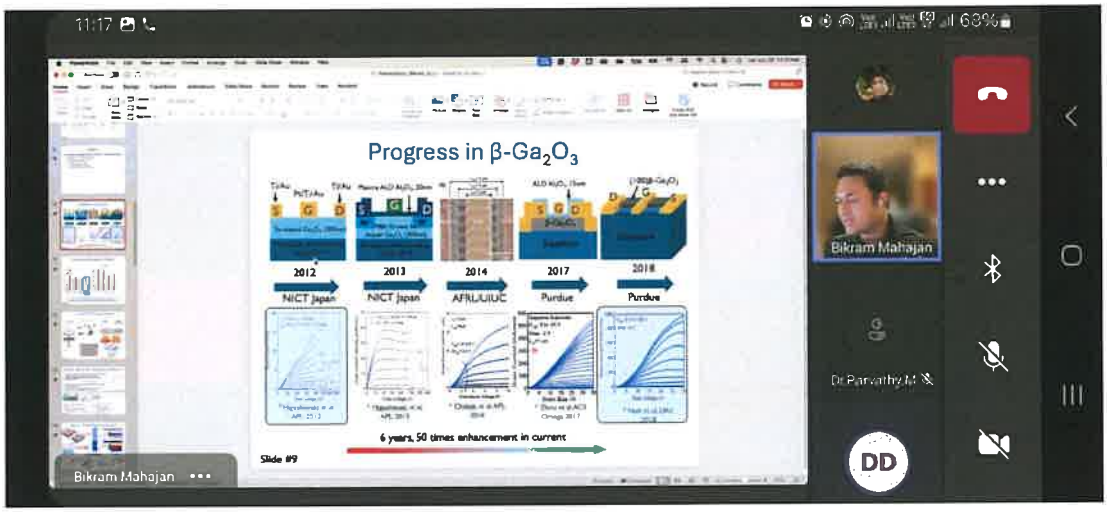
Day-1: 29-06-2024

The first day started with inaugural session including invited talks from Dr. M. Suman (HOD, ECE), Dr. K. Srinivasa Rao (Addl. HOD, ECE), Dr. I. Govardhani (Principal, ASC) and Dr. Aravindhan Alagarsamy (Cohort Head, VLSI), followed by first session from Dr. Bikram K. Mahajan, Purdue University, USA. The topic of speaker was "Electro Thermal Considerations of Wide Band Gap Semiconductors". The speaker for day 1-session 2 was Dr. Pritam Bhattacharjee, VIT Chennai. Dr. Pritam spoke on "Detrimental effects of on-chip power supply noise in modern IC chips".









KL UNIVERSITY

KL Academic Staff College

SHRINKING THE FUTURE

Cutting-Edge Trends in VLSI Design

Faculty Development Program

June 29th – 04th July, 2024

DR. PRITAM BHATTACHARJEE
VIT CHENNAI, INDIA

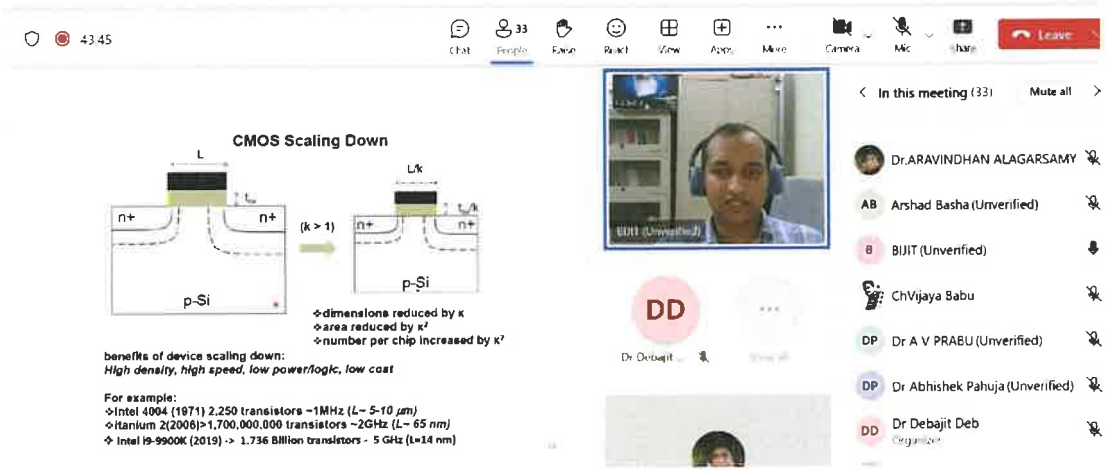
Detrimental Effects of on-chip Power Supply Noise in Modern IC Chips

Session II: 11. 40 AM to 01. 20 PM

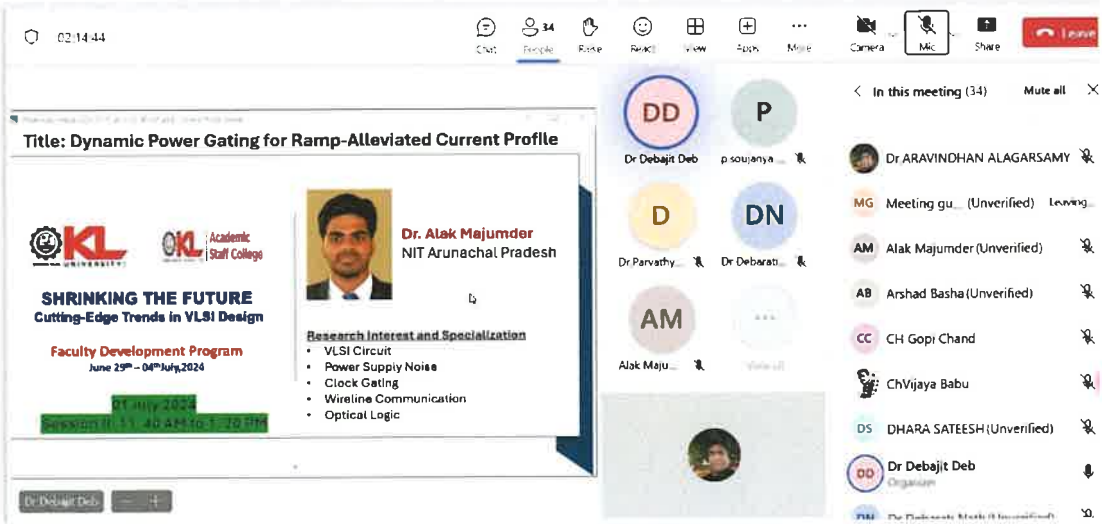
Day-2: 01-07-2024

Day 2 started with an excellent talk on "Evolution of Semiconductor Devices: From P-N junction devices to non-classical Field Effect Transistors" by Dr. Bijit Choudhuri from NIT Silichar. Next session (session 2) of Day 2 was given by Dr. Alak Majumder from NIT Arunachal Pradesh. His title of talk was "Dynamic Power Gating for Ramp Alleviated Current Profile".

Title: Semiconductor Evolution – PN Junction to Non-Classical FET

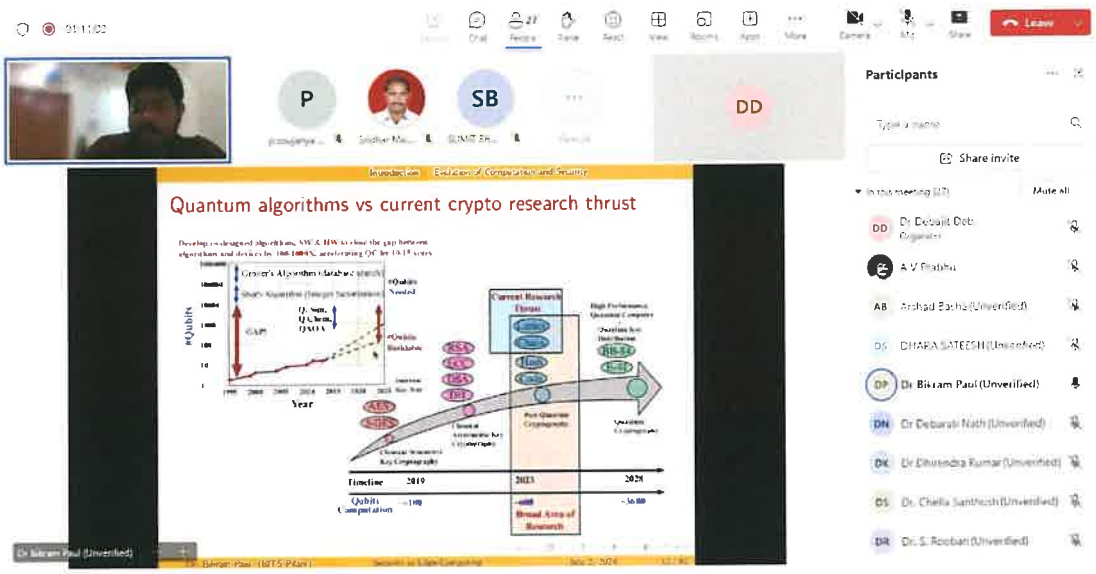


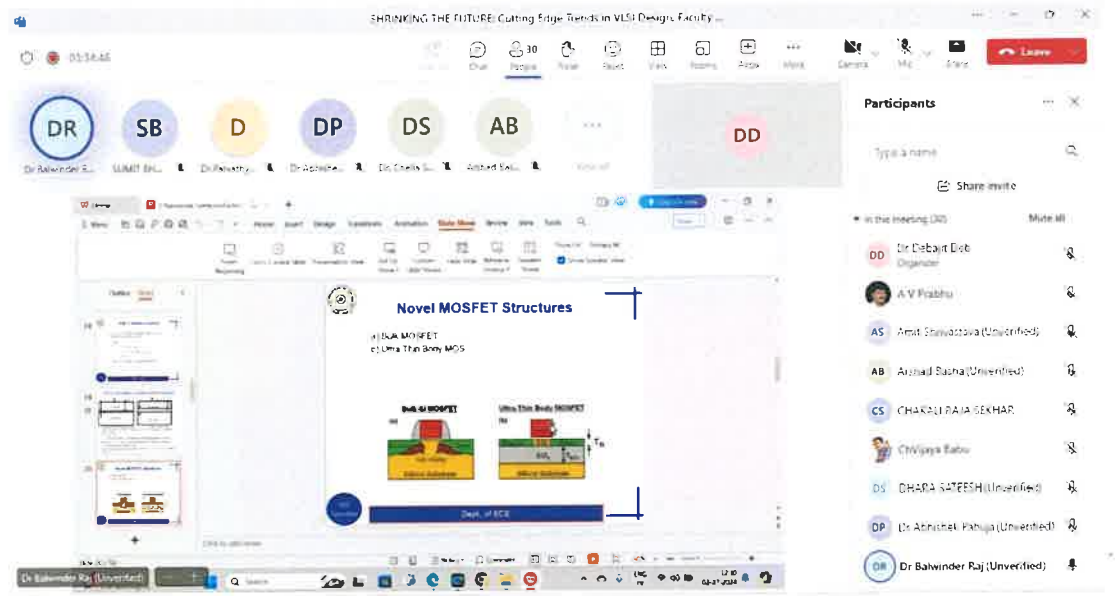
Title: Dynamic Power Gating for Ramp-Alleviated Current Profile



Day-3: 02-07-2024

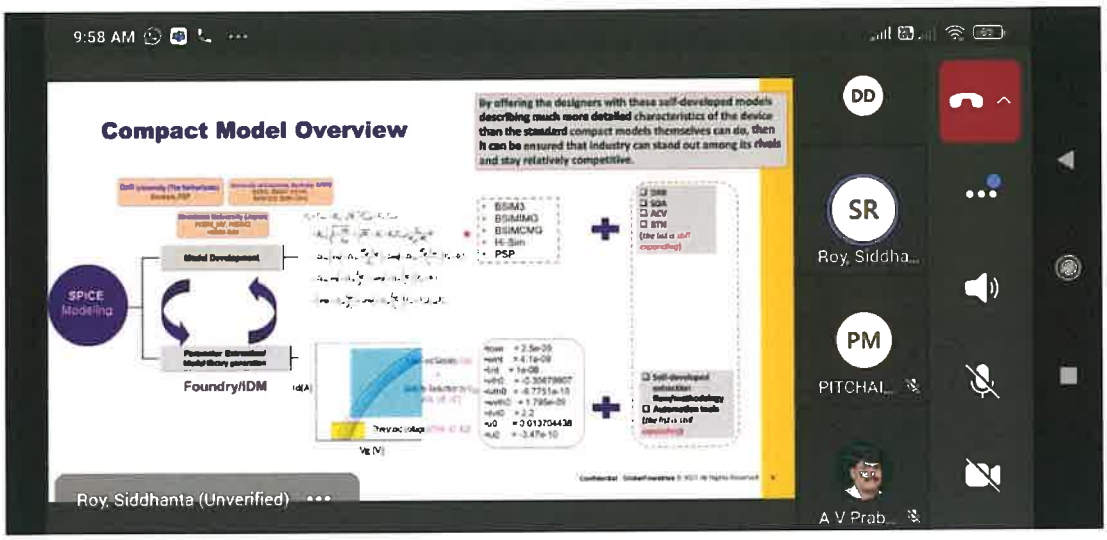
The first session of Day 3 was delivered by Dr. Bikram Paul, BITS Pilani, on "Importance of secure low-power system design for edge computing-based applications". The second session of Day 3 was delivered by Dr. Balwinder Raj from NIT Jalandhar. His topic was "Multi-Gate Semiconductor Devices for VLSI Design". The talk of all resource persons helped the participants to clarify their doubts on multifunctional devices.

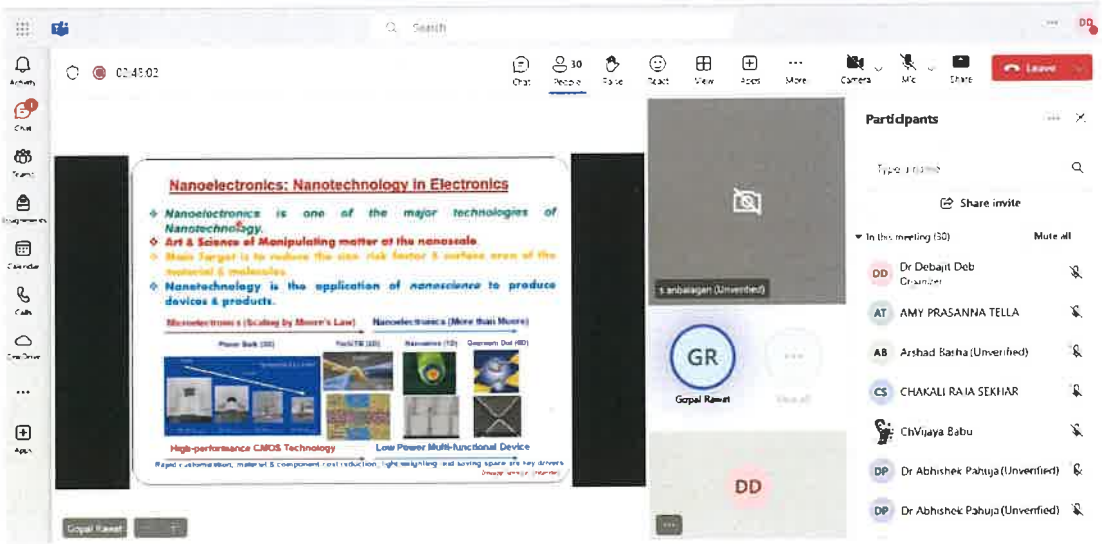




Day-4: 03-07-2024

The first session of day 4 was an industry talk as we all know this will help bridge gap with academia. Dr. Sidhhanta Roy from Global Foundries gave his talk on "Insights on developing compact models and GaN based HEMT technology for power applications". The second session of day 4 was delivered by Dr. Gopal Rawat from IIT Mandi. His talk was on "Design and Fabrication of Nanoelectronic Devices for Sensing Applications."

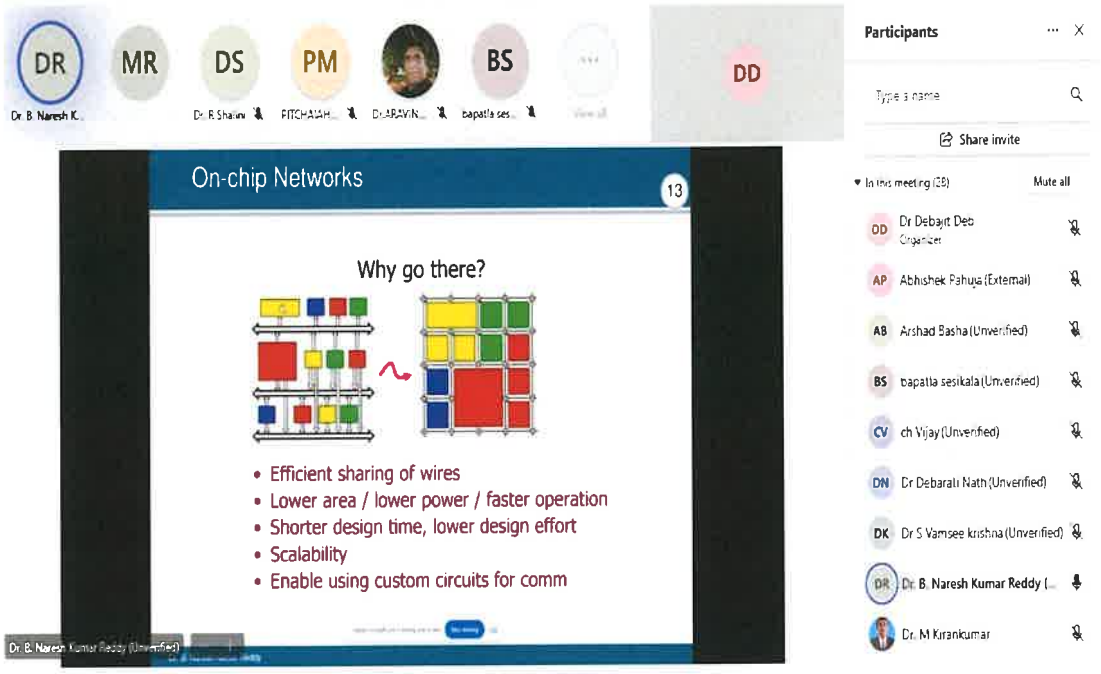


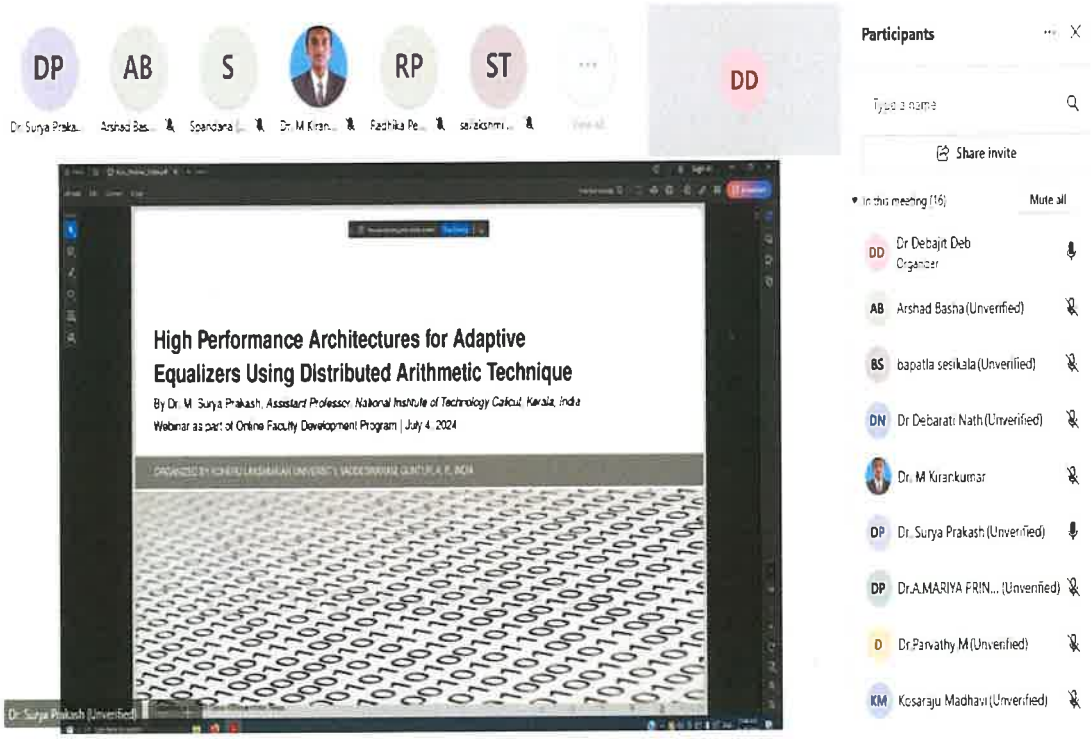


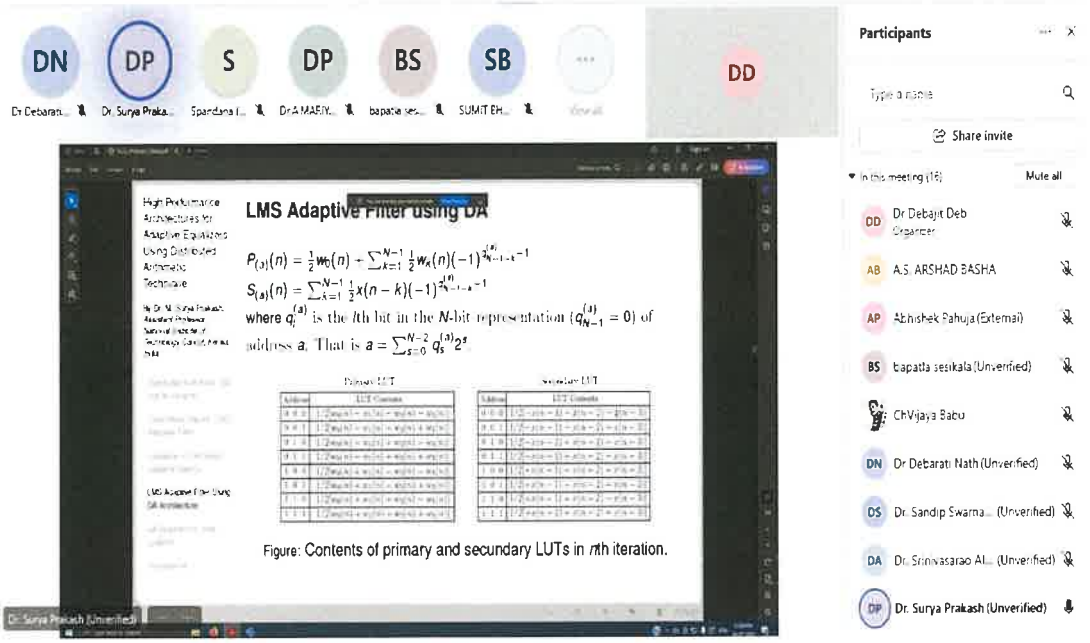
Day-5: 04-07-2024

The first session of Day 5 was delivered by Dr. Naresh K Reddy, NIT Trichy, on "Advancements in Digital Design Techniques and On-Chip Reconfigurable Network Architectures /Design and Implementation of Advanced VLSI Architectures". The second session of Day 5 was

delivered by Dr. M. Surya Prakash from NIT Calicut. His topic was "High Performance Architectures for Adaptive Equalizers Based On Distributed Arithmetic Technique."







The last day of the FDP program ended with a vote of thanks from Dr. Debjit, program convener and Dr. Aravindhan Alagarsamy, Cohort Head, VLSI. Around 95 participants have registered and participated in the program that included faculties, research scholars and other academicians across different parts of the country. They were very active during all sessions and raised their queries to all speakers during interaction round. Overall, the FDP helped all participants to clear their doubts related to the topics of VLSI so that they can implement those concepts both in their academic and research activities.

PRINCIPAL-ASC
9/7/2024

PRINCIPAL
ACADEMIC STAFF COLLEGE
Koneru Lakshmaiah Education Foundation
(Deemed to be University)
Green Fields, VADDESWARAM-522 302