Report on

A One-week National Level Faculty Development Programme (FDP) on

"Low Power MOS Circuit Design and Testing"

Organised by Academic Staff College

In association with Dept. of ECE, KLEF

From 24th to 29th June 2019

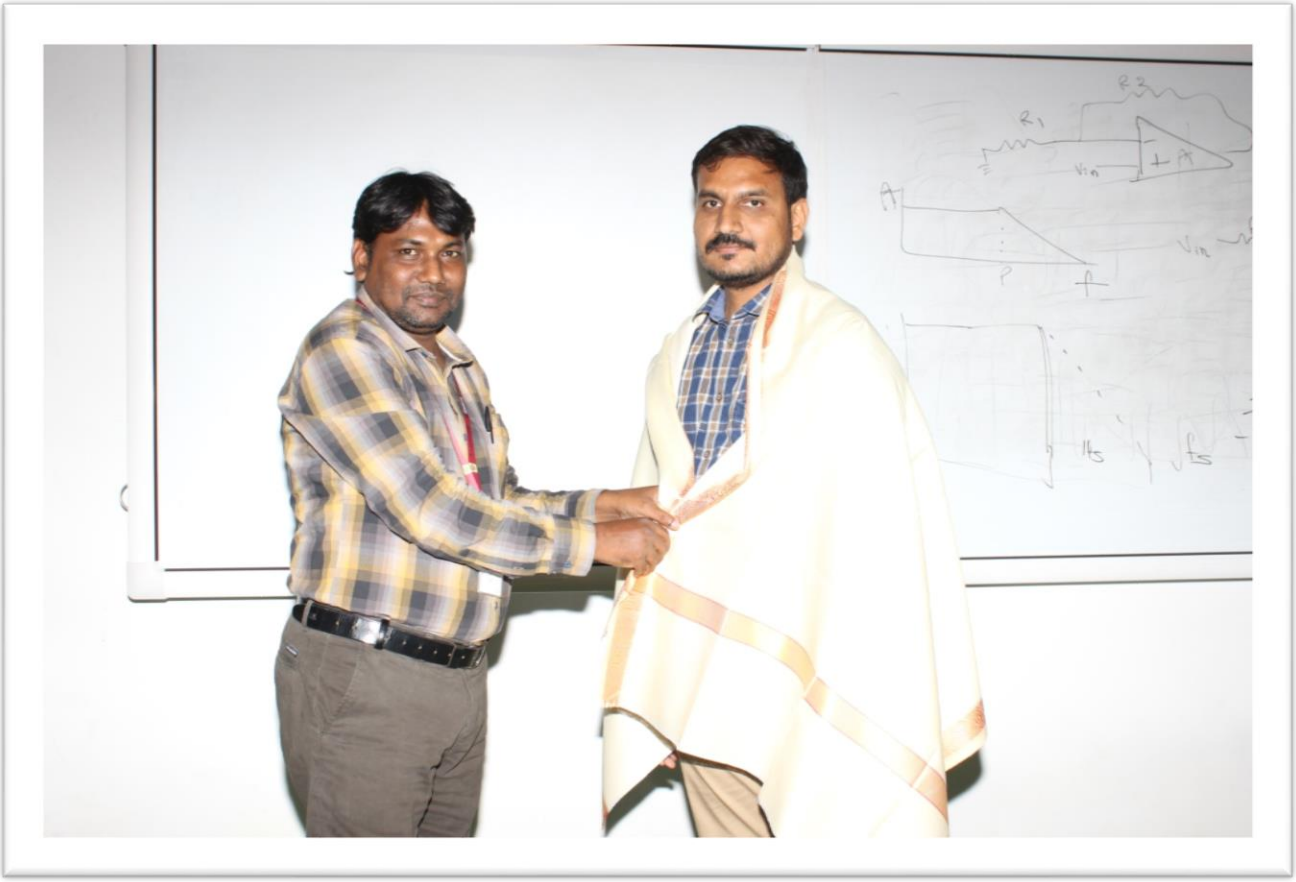
A One-week national level Faculty Development Programme (FDP) on "**Low Power MOS Circuit Design and Testing"**was organised by Academic Staff College in association with Department of ECE, KLEF from 24th to 29th June 2019 for which 45 faculty and scholars across Andhra Pradesh, Telangana, Tamil Nadu had registered and participated in the programme. The FDP was a jointly organised programme by Academic Staff College and Dept. Computer Science and Engineering (CS&E), KL University in association with Electronic & ICT Academy of NIT, Warangal. The FDP was financed by the Ministry of Electronics and Information Technology (MeitY), Govt. of India. Dr.FazalNoorbasha, Associate professor of ECE, KLU was the coordinator for the programme.

Dr.P. SrihariRao, a Professor in School of Electronics and Communication Engineering, NIT Warangal was the chief guest and delivered the inaugural address. While speaking on the occasion,Dr.SrihariRao highlighted that 'Low Power MOS Circuit Design and Testing' is one of the most important areas of research for ECE students and scholars. He added that efficient power management is the need of the hour and advised the faculty to make a note on the numerous methods in power harvesting and its effective management. As part his lecture, **Dr.SrihariRao** dealt with Low Power CMOS circuits.

Further **Dr.SrihariRao**conducted workshop and introduced various methods and approaches through which we can learn the design and optimisation of low power design and its strategies. As part of the FDP Mr.**T I Krishna Readdy** from Texas Instruments from Bangalore dealt with 'An Over View of Low Power VLSI', 'Data Converter Strategies' and 'Low Power and its Testing Strategies'. **Dr. P. Muralidhar**, Professor of ECE from NIT Warangal dealt with 'Low Power Architectures' and another resource person **Mr.NagendraBandi** from Corel Technologies, Hyderabad dealt with the software tools with reference to Low Power VLSI.

Dr. V. Rajesh, Principal, ASC, and Dr. B. Siva Nagaiah Vice-Principal, ASC of KLU had honoured the resource persons with shawls and mementos. Dr.FazalNoorbasha, Associate Professor of ECE and Coordinator of the FDP and Mr. V. VenkataNarayana Dept. ECE had coordinated the FDP.

Resource Person: Mr.Krishna Reddy TI



Resource Person: Dr.Shrihari P NIT, Warangal


KL
CERTIFICATE OF APPRECIATION

Resource Person: Nagendrababu Coreel

Resource Person: Dr.Zia Abbas, IIIT, Hyderabad